

# FABRICATION, CHARACTERIZATION, AND MODELING OF ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

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Initially, advances in the high frequency markets were begun by work in Gallium Arsenide systems. In recent years, however, the focus has shifted to the promise of ever higher power at ever higher frequency with the emergence of wide bandgap group III-V semiconductors, including Gallium Nitride. One area receiving attention is that of novel passivation materials for the active areas of AlGa<sub>N</sub>/Ga<sub>N</sub> devices. Passivation is a critical issue because surface trapping effects are essentially unavoidable, even with the highest quality epitaxial layers, due to the polarized nature of the material. The question then becomes, which passivation materials offer the best mitigation of surface trapping effects with the least impact on parasitic elements detrimental to device performance. In this work, AlGa<sub>N</sub>/Ga<sub>N</sub> devices passivated with AlSi<sub>3</sub>N<sub>4</sub> for both high frequency and high power operation are studied. The high frequency devices were fabricated alongside devices passivated with Si<sub>3</sub>N<sub>4</sub>, a standard passivation material, and characterized for both small signal and large signal performance. The AlSi<sub>3</sub>N<sub>4</sub> passivation was found to enhance both small and large signal performance, and so another set of devices was fabricated with high voltage, high power switching as the intended application. These devices were characterized for off-state breakdown, which was more than 4 times that of typical Si<sub>3</sub>N<sub>4</sub>-passivated devices, and time-domain and loadline measurements were performed.

## **BIOGRAPHICAL SKETCH**

Ekaterina Anatolievna was born in 1985 in Ust'-Ilimsk, Russia. In 1993, her family emigrated to Great Neck, NY, where she attended elementary through high school. She received a Bachelor's of Science with Honors in Electrical Engineering from the California Institute of Technology in 2007. She then entered the Electrical and Computer Engineering M.S/Ph.D program at Cornell University.

For my father.

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# CHAPTER 1

## INTRODUCTION

### 1.1 HEMT Overview

Gallium Nitride (GaN) and Aluminum Gallium Nitride (AlGaN), as well as other group III-V nitrides, have been studied for their high-frequency and high power applications since the early 1990's. A number of review papers are available that chronicle the early development of the technology into the 2000's [5–12]. As the quality of the GaN is dependent on the quality of the substrate on which it is grown, the development of high quality, semi-insulating Silicon Carbide (SiC) substrates was a major breakthrough in GaN-based device processing [13,14]. And while SiC remains the gold standard for high performance GaN devices, recent years have seen Silicon begin to emerge as a low-cost alternative [15,16].

GaN-based devices are especially attractive for high frequency and high voltage operation, and GaN microwave power amplifiers are already commercially available. Because GaN devices have higher power densities and operating voltages than Gallium Arsenide (GaAs) devices, they are particularly attractive for wireless base station applications. State of the art devices have delivered over 30 W/mm of output power at 8 GHz [17], 16 W/mm at 10 GHz [18], and 10 W/mm at 40 GHz [19]. Devices with short gate lengths (30 nm) have shown cutoff frequencies ( $f_T$ ) of 180 GHz [20]. Furthermore, high-efficiency amplifiers have been produced with power-added efficiency (PAE) exceeding 75 % [21].

While the bandwidth of GaN devices is being pushed into ever higher fre-

quencies, power switching at lower frequencies that takes advantage of the high breakdown field of GaN devices is also being explored.

### **1.1.1 High Frequency Applications**

Aluminum Gallium Nitride/Gallium Nitride (AlGaN/GaN) heterostructure high electron mobility transistors (HEMTs) are currently the driving force for high frequency power amplifiers. The AlGaN/GaN HEMT has been studied for its high power handling capability and applications in microwave sources and power amplifiers, as well as monolithic microwave integrated circuits (MMICS) [22–25]. Since their inception, AlGaN/GaN HEMT device performance has steadily improved. Current state of the art devices have delivered over 30 W/mm of output power at 8 GHz [17], 16 W/mm at 10 GHz [18], and 10 W/mm at 40 GHz [19]. Devices with short gate lengths (30 nm) have shown current cut-off frequencies ( $f_T$ ) of 180 GHz [20] and a 60 nm gate device has been reported with a gain cutoff frequency ( $f_{max}$ ) of 300 GHz [15]. Furthermore, high-efficiency amplifiers have been produced with power-added efficiency (PAE) exceeding 75 % [21].

### **1.1.2 Power Switching Devices**

GaN-based devices offer a number of material advantages, including a large bandgap which results in high breakdown field and high power density. Furthermore, the AlGaN/GaN system forms a spontaneous, confined 2-dimensional electron gas (2DEG) without doping. This 2DEG has a high sheet

charge, which translates directly to large current densities. Because there is also less impurity scattering, the saturated drift velocity of GaN is relatively large, which means a high saturation current. This all translates into high voltage and high current operation, meaning high efficiencies and high power density per unit area. It is for these reasons that the GaN material system is ideal for power switching and power amplifier devices. High efficiency and low power loss mean lower cooling costs, a major issue for modern wireless communication systems, which require high efficiency to reduce energy consumption and improve reliability.

One goal of power switch research is to take full advantage of these material properties to obtain the highest possible breakdown voltage for the device. In recent years, the upper limit for off-state breakdown voltage has been continually pushed from a few hundred volts into the kilovolt range [26–29]. Record breakdown voltages of 1900 V [30] and 2200 V [31] have been reported for traditional HEMT layouts, and Tsurumi *et al* reported a novel via drain structure on SiC with a breakdown of 10400 V [32]. Many of these high breakdown voltage devices mentioned above share a few common characteristics: long ( $> 1 \mu\text{m}$ ) gate lengths, large gate drain spacings ( $> 10 \mu\text{m}$ ), and typically one or more field plates.

Recently, there has been a trend toward GaN-on-Si for power switching applications, as the high frequency performance of substrates like SiC can be traded off for lower costs and high volume production [16, 33, 34]. Much of this shift can be attributed to advances in the growth of good quality AlGaIn/GaN films on 4" and 6" (111) Si substrates [35]. While GaN-on-Si technology faces a number of challenges, which include off-state leakage current and high dy-



dynamic on-resistance, device breakdown voltages on par with those of devices grown on SiC have been realized [36].

## **1.2 Summary of Thesis**

This work is divided into 6 chapters. Chapter 2 is a brief overview of the material properties of GaN-based devices, device physics, the formation of the 2DEG, as well as a detailed description of the fabrication process. Chapter 3 briefly discusses basic device measurements and test bench setups. Chapter 4 discusses the device small signal model in detail. Chapter 5 presents the results of a passivation study comparing AlSiN and SiN passivation schemes, with both small- and large-signal results. Chapter 6 describes AlSiN-passivated devices for power switching applications.

## CHAPTER 2

### DEVICE PHYSICS AND FABRICATION

#### 2.1 Device Physics

In order to understand basic device physics, a certain knowledge of the properties of the material system in which one is working is required. The study of the growth of quality GaN and the investigation of its material properties, as well as the study of the AlGaIn/GaN system, is well-covered in literature and still ongoing [37–41].

##### 2.1.1 Structure

Gallium Nitride, along with other group III nitrides such as AlN and InN, has several possible crystal configurations. Namely, these nitrides can grow as zincblende, wurtzite, or rocksalt. However, it is the wurtzite configuration that is most typically seen, as it is the structure that is stable at room temperature [42], as well as the structure that forms during high temperature growth. The wurtzite configuration is also responsible for the spontaneous polarization observed in group III nitrides.

The wurtzite crystal consists of two overlapping hexagonal close packed lattices, with the Ga and N forming tetragonal bonds. The crystal can be grown as either Ga or N face [2, 43]. Figure 2.1 shows the two overlapping hcp lattices of wurtzite, and in the case of GaN this particular arrangement would be N-face. What makes the wurtzite structure of GaN, and other column III ni-

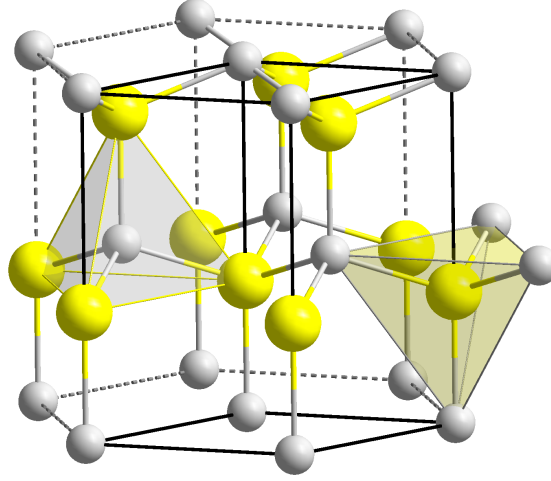


Figure 2.1: The wurtzite lattice structure of GaN, showing a nitrogen face.

trides, interesting is that the wurtzite structure lacks higher symmetry. Whereas zincblende's ABCABC stacking sequence produces a higher order cubic symmetry, wurtzite's ABABAB sequence does not, and therefore produces a unique c-axis along (0001). The bond along the c-axis is longer than the other three bonds, which leads to spontaneous polarization along the c axis [44].

### 2.1.2 Material Properties

While a number of techniques have been used to grow bulk single crystal GaN in recent years, most processes still suffer from high dislocation rates and imperfections such as etch pitting [45–47]. Therefore, heteroepitaxy is still the most common method of producing thick GaN layers. Historically, GaN has been grown on either SiC or sapphire. GaN-on-Si [48–51] and GaN-on-diamond [52–55] technologies have been maturing in recent years and may prove to be possible avenues for both cheaper (Si) and higher performance (diamond) appli-

cations. Between sapphire and SiC, SiC is preferred owing to its higher thermal conductivity (4.9 W/cm·°K vs sapphire's 3.5) and smaller lattice mismatch to GaN (3 %, versus 13 % for sapphire). The smaller mismatch allows for growth of higher quality GaN. Furthermore, SiC has a much higher thermal conductivity than sapphire, which allows for better thermal management in high power applications. Sapphire, however, is much cheaper and available in larger wafers. Table 2.1 summarizes the electrical and thermal properties of GaN, GaAs, Si and SiC.

Table 2.1: Electrical and thermal properties of GaN, GaAs, Si and SiC, from [1]

Material	$E_g$ [eV]	$\epsilon$	$\mu$ [cm <sup>2</sup> /V·s]	$E_c$ [MV/cm]	$v_{sat}$ [10 <sup>7</sup> cm/s]	Thermal Conductivity [W/cm·°K]
Si	1.1	11.4	1300	0.3	1	1.5
SiC	3.2	9.7	800	2	2	4.9
GaAs	1.4	13.1	6000	0.4	1	0.46
GaN	3.4	9.5	1500	3.3	1.5	1.7

One advantage of GaN over GaAs becomes immediately clear—GaN (and SiC) has almost three times the bandgap of GaAs and Si. A large bandgap translates into high critical electrical fields, which ultimately allows for large operating and breakdown voltages. This also allows for higher output power per unit width, which means smaller devices with large power densities. High operating voltages also mean that it is unnecessary to step down the voltage for certain commercial applications, such as wireless base stations that operate at 28 V.

### 2.1.3 2DEG formation

The AlGaIn/GaN heterostructure exhibits both spontaneous and piezoelectric polarization. As discussed earlier, the wurtzite structure of group III nitrides lacks higher order symmetry which, combined with the non-covalent nature of the bonds between neighboring Ga and N atoms, produces an asymmetrically long bond in the (0001), or c-axis. This, in turn, produces a spontaneous polarization along the c-axis, denoted by  $P_p$ . The direction of the polarization depends on which face of the crystal is at the surface. Furthermore, the strength of the polarization field is enhanced as the ratio of the lattice constants strays from that of an ideal hcp lattice (1.633).

Table 2.2: Spontaneous polarization, structural, and piezoelectric constants of several group III nitrides [2, 3].

Parameter	GaN	InN	AlN
$P_{sp}$ [C/m <sup>2</sup> ]	-0.029	-0.032	-0.081
$c_0/a_0$	1.6259	1.6116	1.6010
$e_{31}$ [C/m <sup>2</sup> ]	-0.49	-0.57	-0.60
$e_{33}$ [C/m <sup>2</sup> ]	0.73	0.97	1.46

Bernardini et al [3] described the piezoelectric polarization that occurs in group III-nitrides under strain. In the ternary compounds, such as AlGaIn, the strain is controlled by the lattice mismatch at the AlGaIn/GaN interface. The mismatch in the  $a_0$  lattice parameters results from the presence of Al, and the amount of strain can be controlled by tuning the Al fraction. The vector is calculated as [2]

$$P_{pz} = 2 \frac{a - a_0}{a_0} \left( e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right)$$

Table 2.2 shows the magnitude of the spontaneous polarization for several group III-nitrides and the structural and piezoelectric constants used to calculate the magnitude of the piezoelectric polarization.  $C_{11}$  and  $C_{33}$  are elastic constants.

Knowing the magnitudes of these polarization vectors allows us to determine the state of the interface between AlGaN and GaN.

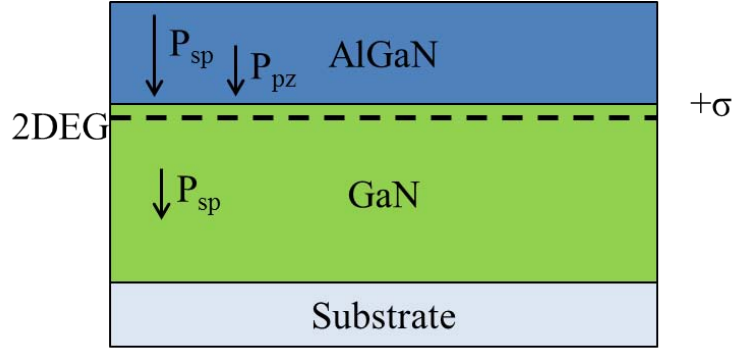


Figure 2.2: Typical AlGaN/GaN heterojunction with polarization vectors. The 2DEG forms during growth as electrons migrate from the bulk to offset the bound positive charge at the interface.

Figure 2.2 shows a typical AlGaN/GaN heterojunction, with Ga-face GaN. Usually, the GaN layer is relatively thick (1-2  $\mu\text{m}$ ), while the AlGaN layer is thinner, on the order of tens of nanometers. Because AlN has a larger spontaneous polarization vector than GaN, the ternary AlGaN naturally has a vector that is larger than GaN. Furthermore, because the AlGaN is thin, it is under tensile strain, creating a piezoelectric polarization vector which points in the same direction as the spontaneous polarization vector.

We can now apply Gauss's law (the gradient of the total polarization is re-

lated to the bound charge) to the interface:

$$\vec{\nabla} \cdot \vec{P} = -\rho_{\text{bound}}$$

First, since both  $P_{sp}$  and  $P_{pz}$  point in the same direction, the total polarization is their sum.

$$\sigma^{\text{AlGaIn}} = -P^{\text{AlGaIn}} = -(P_{sp}^{\text{AlGaIn}} + P_{pz}^{\text{AlGaIn}})$$

$$\sigma^{\text{AlGaIn/GaN}} = P^{\text{AlGaIn}} - P^{\text{GaN}} = (P_{sp}^{\text{AlGaIn}} + P_{pz}^{\text{AlGaIn}}) - P_{sp}^{\text{GaN}}$$

And since the sum of  $P_{sp}^{\text{AlGaIn}}$  and  $P_{pz}^{\text{AlGaIn}}$  is necessarily greater than the  $P_{sp}$  of GaN, we get a positive bound charge at the interface.

This positive sheet charge attracts free carriers from the bulk, resulting in a 2DEG. The 2DEG that forms from the positive sheet charge is now confined to the interface due to the conduction band offset between the GaN and AlGaIn (Figure 2.3).

The carrier sheet density can then be calculated [4]:

$$n_s = \frac{1}{q} \frac{\sigma^{\text{AlGaIn/GaN}} - c_{\text{AlGaIn}}(\phi_b - \Delta E_c) - c_{\text{GaN}}\phi}{1 + c_{\text{AlGaIn}} \frac{\pi \hbar^2}{q^2 m^*}}$$

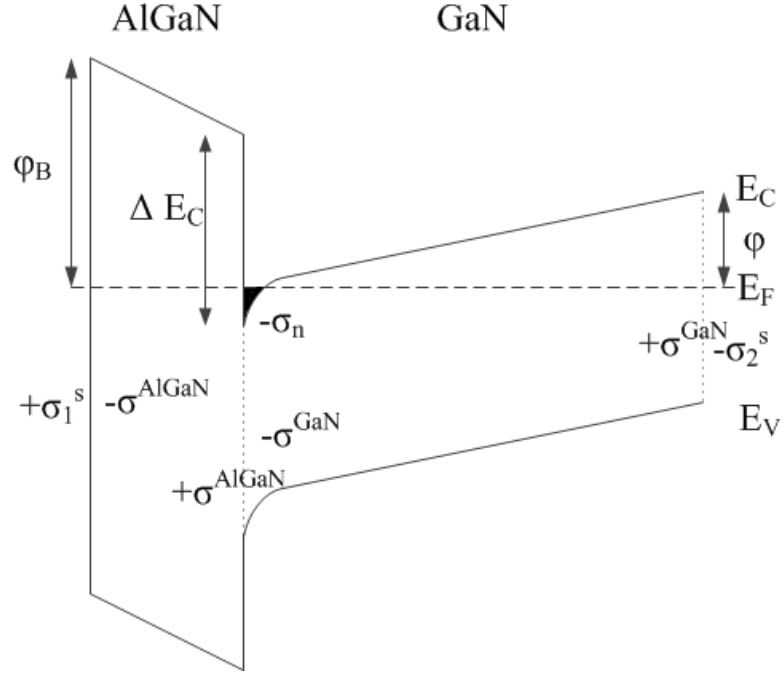


Figure 2.3: Band diagram of the AlGaN/GaN interface, showing the band-bending that results from the conduction band offset  $\Delta E_c$ , the barrier height  $\phi_b$ , and surface potential  $\phi$ , after Prunty et al [4].

## 2.2 HEMT Fabrication

Figure 2.4 shows a cross-section schematic of each step of the HEMT fabrication process. Device fabrication begins with a 13 x 13 mm piece of heteroepitaxially grown AlGaN/GaN structure (Figure 2.4(a)). The first step is the mesa/alignment layer, which contains the alignment marks for electron-beam lithography, stepper and contact photolithography, and mesa isolation pattern. This layer is defined by photolithography using Shipley Positive Resist (SPR) 955-0.9 and exposure in the GCA Autostep. The mesa layer is etched using a  $\text{Cl}_2/\text{BCl}_3/\text{Ar}$  plasma etch (Figure 2.4(b)). The photoresist is removed with a combination of 1165 resist strip soak and a two minute, 200 °C oxygen plasma ash.



The surface is then cleaned with HCl, and the passivation layer is grown by LPCVD at 750 °C (Figure 2.4(c)). A three layer stack is spun for e-beam lithography: an AR3 (anti-reflecting) layer, LOR 5A as the metal lift-off layer, and UV 210-0.6 resist. The stack is coated with 15 nm of Al to serve as a conducting layer for e-beam lithography. Ohmic windows are defined, and etched using either  $\text{CHF}_3/\text{O}_2$  or  $\text{SF}_6/\text{Ar}$  plasma for AlSiN and SiN, respectively (Figure 2.4(d)). The windows are cleaned in 1:1 HCl, and the ohmic metal stack of V/Ti/Al/Mo/Au is deposited by e-beam evaporation (Figure 2.4(e)). Lift-off is performed by soaking in 1165 resist strip, and the AR3 layer is removed by ashing. A thin (20 nm) SiN cap is deposited by PECVD at 300 °C (Figure 2.4(f)). This cap retains the shape of the ohmic metal stack and prevents it from creeping during the anneal, which is performed using a rapid thermal annealer (RTA) at 850 °C for 1 minute.

To define a “t” or “mushroom” gate, a stack of dielectrics is deposited. First, and approximately 75-100 nm layer of AlN is deposited by DC sputter deposition. Then, an approximately 100-120 nm layer of SiN is grown by PECVD (Figure 2.4(g)). Finally, a 20 nm conducting layer of Ti is deposited by e-beam evaporation. ZEP 520 resist thinned 1:2 in Anisole is spun, exposed, and developed. The gate is defined by a series of dry reactive-ion etches (RIEs) through the dielectric/metal stack. The Ti and AlN layers are etched with  $\text{BCl}_3/\text{Ar}$ , and both of the PECVD SiN layers are etched with  $\text{SF}_6/\text{Ar}$ . Lastly, the passivation layer is etched with  $\text{SF}_6/\text{Ar}$  (Figure 2.4(h)). The sample is then annealed at 700 °C for 1 minute to heal the etched surface.

For the gate metal, a bilayer of 495 and 950 weight polymethylmethacrylate (PMMA) is spun, and a conducting layer of Al (15 nm) is evaporated. The gate

metal is defined by e-beam lithography, the Ni/Au Schottky gate is deposited by e-beam evaporation, and lift-off in methylene chloride is performed (Figure 2.4(i)). At this point, the AlN layer may be removed by soaking in basic photoresist developer to define the t-gate.

Contact pads are defined on an LOR 10A/SPR 955-0.9 bilayer by photolithography, and windows through the ohmic cap are etched by  $\text{SF}_6/\text{Ar}$  plasma (Figure 2.4(j)).

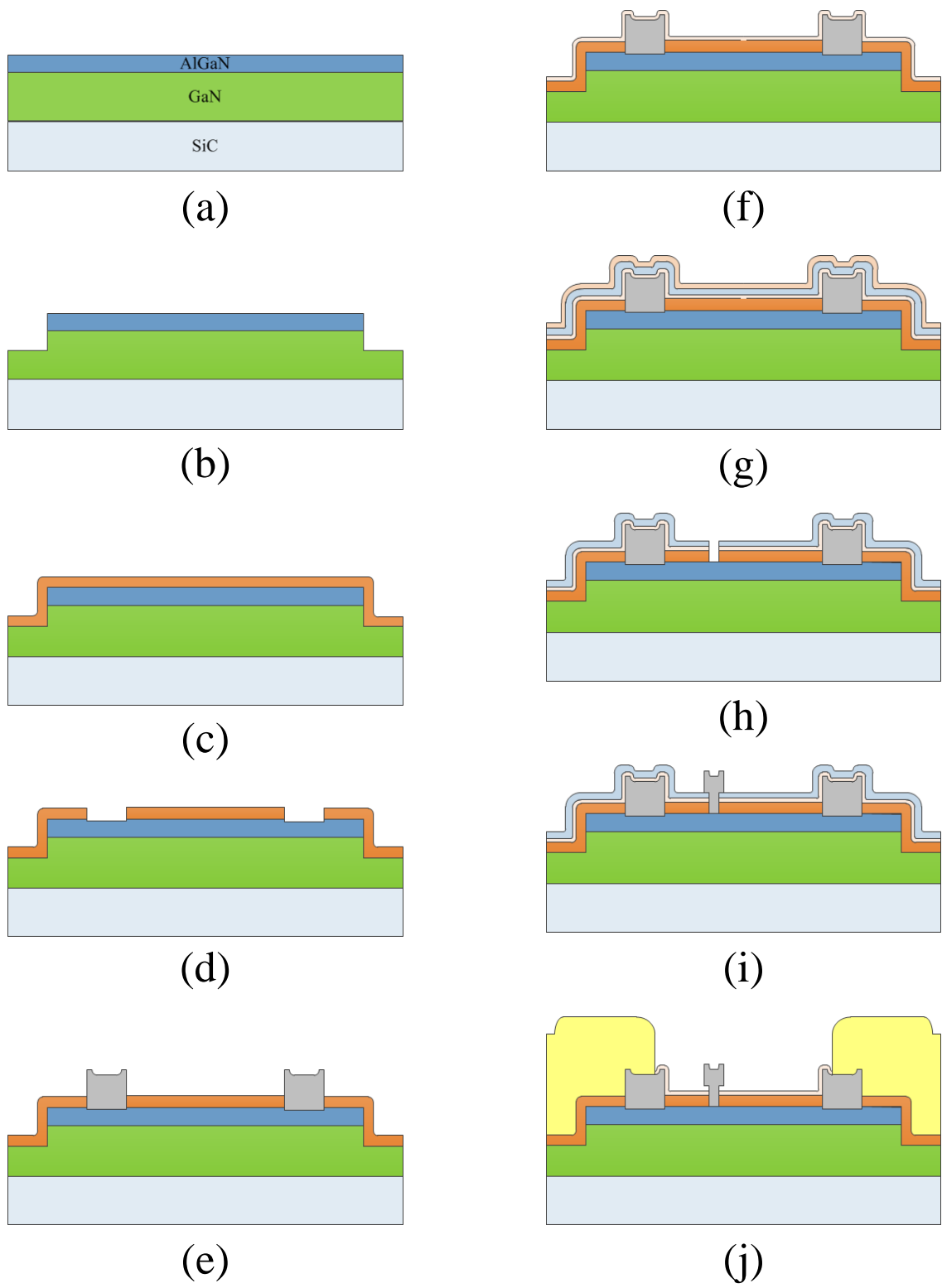


Figure 2.4: Standard HEMT fabrication process.

## CHAPTER 3

### CHARACTERIZATION

#### 3.1 DC

The DC portion of the the standard characterization procedure involves primarily the transfer curve and family of output curve measurements. These simple initial tests provide basic parameters, such as pinch-off voltage, DC transconductance, and knee voltage, which are subsequently used in small and large signal characterization and device modeling.

##### 3.1.1 Transfer Curves

The first set of measurements taken on every device is the drain current versus gate bias measurement, or transfer curve. The drain is biased at a fixed voltage, usually 15 V, and the gate is swept from some negative value beyond pinch-off into forward bias so that the device turns on. If necessary, the bias may be extended to observe the full channel saturation current, though this is not done for every measurement. This measurement immediately yields the pinch-off voltage of the device. This is the (usually negative) bias that must be applied to the gate to repel carrier from the channel, thus preventing the channel from conducting.

The transconductance can then be derived from this measurement. The DC transconductance is defined as the derivative of the drain current with respect to gate voltage:

$$g_m^{DC} = \frac{dI_{ds}}{dV_{gs}}$$

Note that this is the DC transconductance, which is often different from the RF transconductance due to dispersion [56]. The transconductance plot yields an important bias point, which will be referred to at  $V_{gs}^q$ . This is the value of the gate bias where the transconductance is at its peak, and will be used as the gate bias at which the small signal parameters of the device are extracted.

Figure 3.1 shows a typical set of transfer curves for a device with a 400  $\mu\text{m}$  gate periphery and 1  $\mu\text{m}$  gate length.

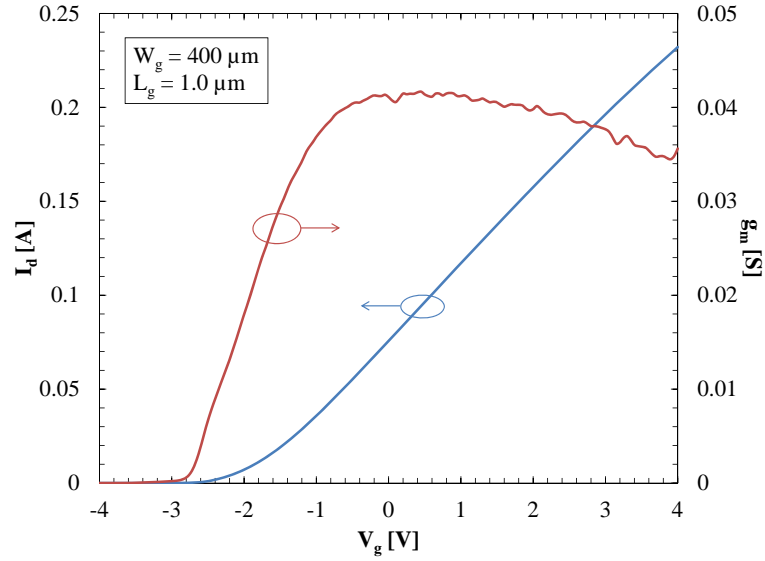


Figure 3.1: Typical transfer curves—drain current and transconductance versus gate bias—of a 400  $\mu\text{m}$  gate periphery, 1  $\mu\text{m}$  gate length device. The drain was biased at 15 V.

During this measurement, the gate current is also recorded. This is used to check for and compare gate leakage across devices. Since the source measurement units (SMUs) provide at 1 M $\Omega$  shunt, the measured gate current must be corrected to account for shunt resistor. Figures 3.2 and 3.3 show a typical

gate current measurement for a  $400\text{ }\mu\text{m}$  gate periphery device on linear and log scales, respectively.

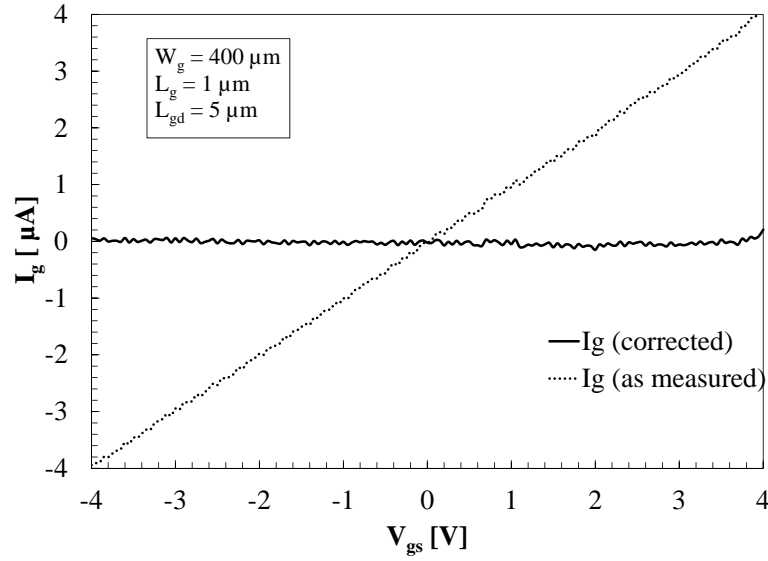


Figure 3.2: Typical transfer curves—drain current and transconductance versus gate bias—of a  $400\text{ }\mu\text{m}$  gate periphery,  $1\text{ }\mu\text{m}$  gate length device.  $V_{ds} = 15\text{ V}$ .

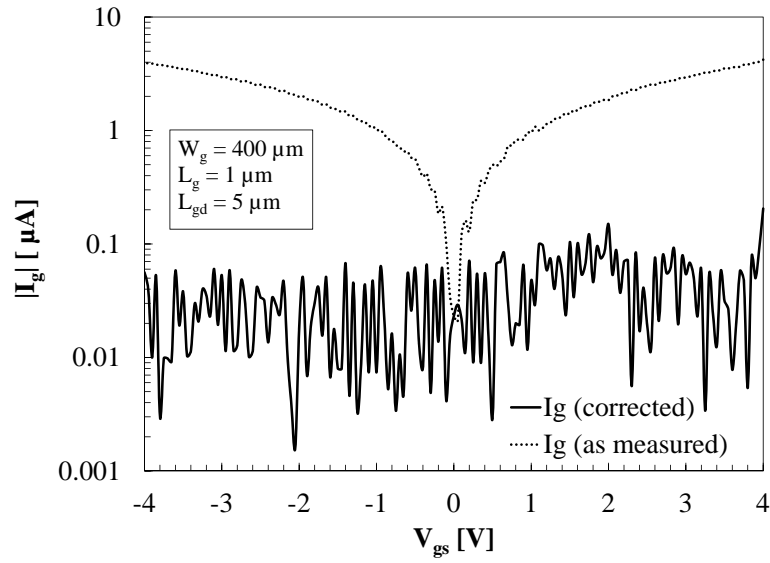


Figure 3.3: Typical transfer curves—drain current and transconductance versus gate bias—of a  $400\text{ }\mu\text{m}$  gate periphery,  $1\text{ }\mu\text{m}$  gate length device.  $V_{ds} = 15\text{ V}$ .

### 3.1.2 Output Curves

A family of output curves is measured to find the knee voltage, on-resistance, and DC output conductance. This is done by stepping the gate voltage from just beyond pinch-off to a value that yields full channel current, and sweeping the drain voltage from 0 to 10 V.

## 3.2 Small Signal

This section describes the methodology of small signal measurements and the metrics derived thereof. “Small signal” refers to the fact that the perturbation of the input signal is small and the response is assumed to be linear. This is in contrast to power, or “large signal” measurements which rely on large driving signals and exhibit a good deal of non-linearity.

### 3.2.1 S-Parameters

High frequency measurements of networks present a problem when attempting to take direct measurements in the form of the magnitude and phase of a signal, and attempting to discern the voltage, current, and associated impedances or admittances. Instead, the scattering matrix is often used, as it completely describes the reflected and transmitted waves, and thus the network, in a practical way. S-parameters offer a number of advantages, including simple conversion to Z, Y, and ABCD parameters, as well as being used directly in the calculation of network metrics like gain and cutoff frequencies [57]. Furthermore, S-parameter

measurements are extremely useful in shifting reference planes, and thus almost universally used for calibrating Vector Network Analyzers. For an  $n$ -port network, the scattering matrix is defined by the ratios of incident ( $V_n^+$ ) and reflected ( $V_n^-$ ) voltage waves as [57]:

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1n} \\ S_{21} & & & \vdots \\ \vdots & & & \\ S_{n1} & \dots & & S_{nn} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_n^+ \end{bmatrix}$$

For a 2-port network, this can be written as:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+=0} & \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+=0} \\ \left. \frac{V_1^-}{V_2^+} \right|_{V_1^+=0} & \left. \frac{V_2^-}{V_2^+} \right|_{V_1^+=0} \end{bmatrix}$$

### 3.2.2 Small Signal Metrics

#### Unity Gain Cutoff Frequency ( $f_T$ )

The current unity gain cutoff frequency,  $f_T$ , is also known as the transition frequency. This metric indicates the speed at which the electrons traverse the channel, and can be defined as:

$$f_T = \frac{v_{eff}}{2\pi L_{eff}}$$

Thus, knowing the cutoff frequency and channel length, we can estimate the effective velocity of the electrons. Typically,  $f_T$  is determined by plotting the magnitude of the current gain, which is conveniently represented by the hybrid



parameter  $h_{21}$ . The hybrid parameters can be directly measured with a vector network analyzer, or easily derived from either S- or Y-parameters:

$$h_{21} = \frac{Y_{21}}{Y_{11}} = \frac{-S_{21}}{(1 - S_{11})(1 + S_{22} + S_{21}S_{12})}$$

This parameter is usually plotted on a log scale frequency scale in dB, and if it does not cross the x-axis, the cutoff frequency is extrapolated by assuming a -20dB/decade slope from the last points. Figure 3.4 is a typical  $|h_{21}|$  plot derived from Y-parameter measurements of a 100  $\mu\text{m}$  gate width, 0.15  $\mu\text{m}$  gate length device, and shows an approximately 80 GHz  $f_T$ .

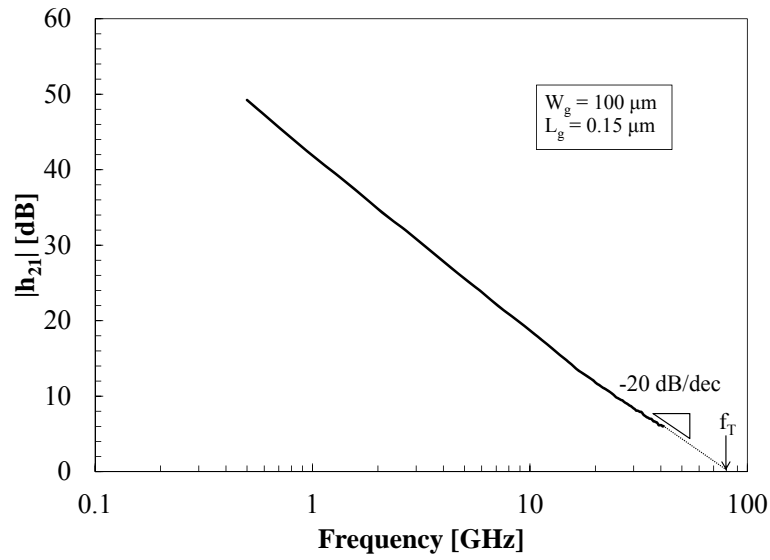


Figure 3.4: Typical  $h_{21}$  parameter measurement of a 100  $\mu\text{m}$  gate periphery, 0.15  $\mu\text{m}$  gate length device. The cutoff frequency  $f_T$  is extrapolated by assuming a -20dB/decade slope. In this case, it is approximately 80 GHz.

### Stability and Unity Power Gain Cutoff Frequency ( $f_{max}$ )

Before discussing power gain, it is important to briefly mention stability. Because a device may be prone to oscillation at certain frequencies, it is important to differentiate the maximum *stable* gain of a device from the maximum *available* gain. One common test for unconditional stability is Rollet's test [57], where Rollet's constant  $k$  must be greater than 1:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

and also,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

When Rollet's condition is satisfied, the term *maximum available gain* is used to describe the gain of such an unconditionally stable device, and is calculated as:

$$MAG = \frac{|S_{21}|}{|S_{12}|} (k - \sqrt{k^2 - 1})$$

When  $k < 1$ , the device is considered conditionally stable. Due to the possibility of oscillation, the term *maximum stable gain* is used to describe the gain, and may be calculated by substituting  $k = 1$  into the equation for maximum available gain, giving:

$$MSG = \frac{|S_{21}|}{|S_{12}|}$$

Figure 3.5 shows a typical MSG/MAG plot of a 100  $\mu\text{m}$  gate width, 0.15  $\mu\text{m}$  gate length device. Note the point at which  $k$  "breaks", and the device becomes

unconditionally stable. The point at which MAG is unity (0 dB) is called the unity power gain cutoff frequency, or  $f_{max}$ . If MAG does not cross the x-axis,  $f_{max}$  is extrapolated like  $f_T$ , by drawing a -20 dB/dec line.

Figure 3.5 shows the

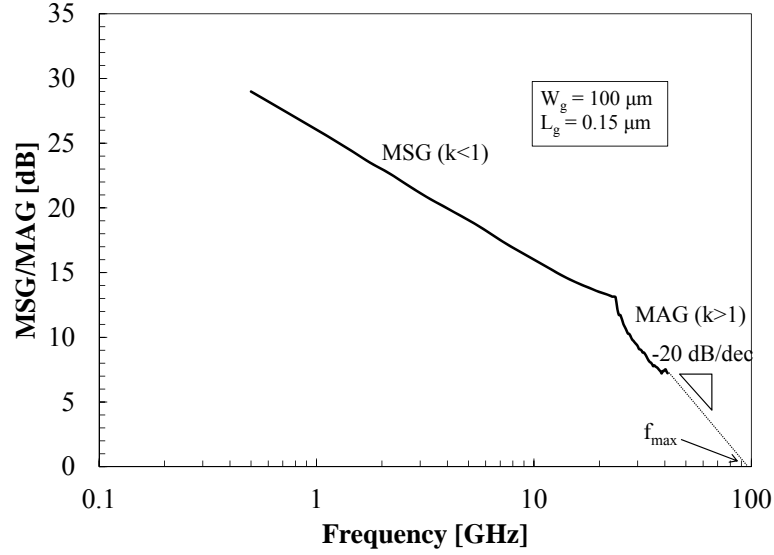


Figure 3.5: Typical MSG/MAG plot of a 100  $\mu\text{m}$  gate periphery, 0.15  $\mu\text{m}$  gate length device. The transition from unstable to stable gain is shown where  $k = 1$ . The cutoff frequency  $f_{max}$  is extrapolated by assuming a -20dB/decade slope. In this case, it is > 90 GHz.

### 3.3 Large Signal

#### 3.3.1 Load pull setup

The methodology described in this section appears in [58]. A schematic of the large-signal measurement system is given in Figure 3.6.

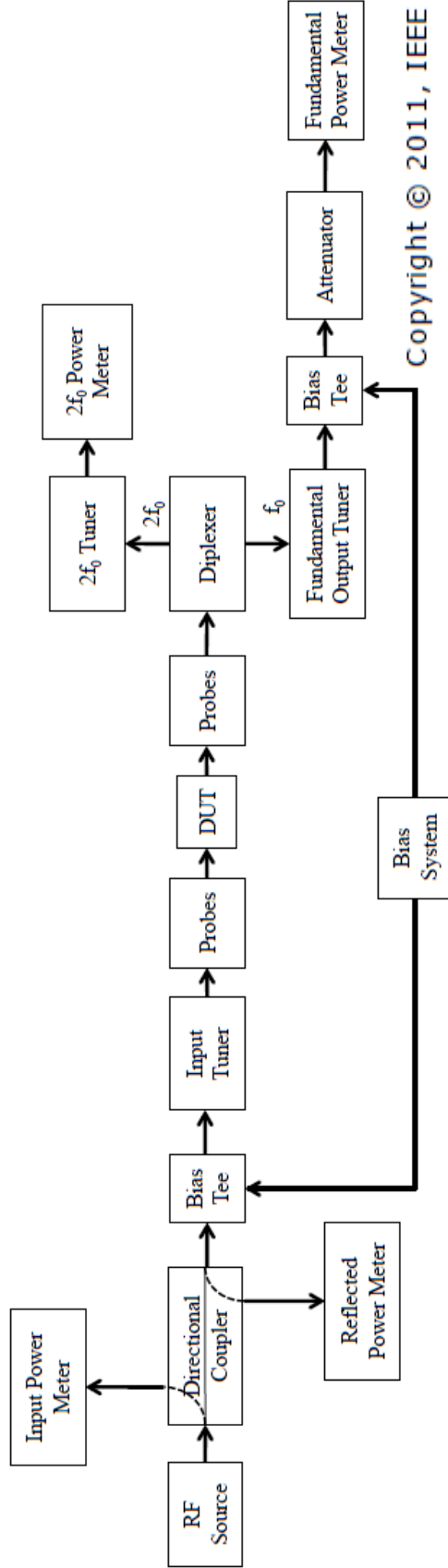


Figure 3.6: Schematic of large signal power bench featuring a low loss diplexer to separate the 10 and 20 GHz components of the output signal.

The 10 GHz signal is generated by an Agilent 83650 CW generator and then amplified with a 10 W amplifier. Bias is supplied by an Agilent 4142B SMU through bias tees at the input of the input tuner and the output of the fundamental output tuner. Maury MT982 mechanical tuners are used as the input and fundamental output tuners, and one MT983 tuner is used for the second harmonic output. The fundamental and second harmonic outputs signals are separated by a diplexer with measured insertion loss of 0.21 dB. The fundamental output signal is attenuated by a 30 dB attenuator after the output tuner. The input and reflected signals are measured with an Agilent E4417A dual-channel power meter. A second Agilent E4417 is used to measure the fundamental and second harmonic output powers. The bench is calibrated using an HP 8510C, 50 GHz network analyzer. Each section of the setup, starting with each path in the directional coupler, is calibrated separately by measuring the s-parameters. This allows us to later transform the signal to the device plane.

The first step of the matching process is setting the source impedance. The goal is to create a conjugate match to allow maximum power transfer from the source to the device. Therefore, the reflected power should be minimized. The matching is done by first scanning the input tuner slide over the range of a wavelength to find the point where the reflected power is at a minimum. Then, the probe is scanned and again the point of minimum reflected power is taken. If it is necessary to verify a conjugate match, the connection may be broken between the output of the input tuner and the input probes. Keeping all other connections, the one-port s-parameters can be measured for the input into the device using the input probes, and the output of the input tuner looking backwards toward the source. These two sets of  $s_{11}$  measurements can then be transformed to the device plane and mapped on a Smith chart (Figure 3.7).

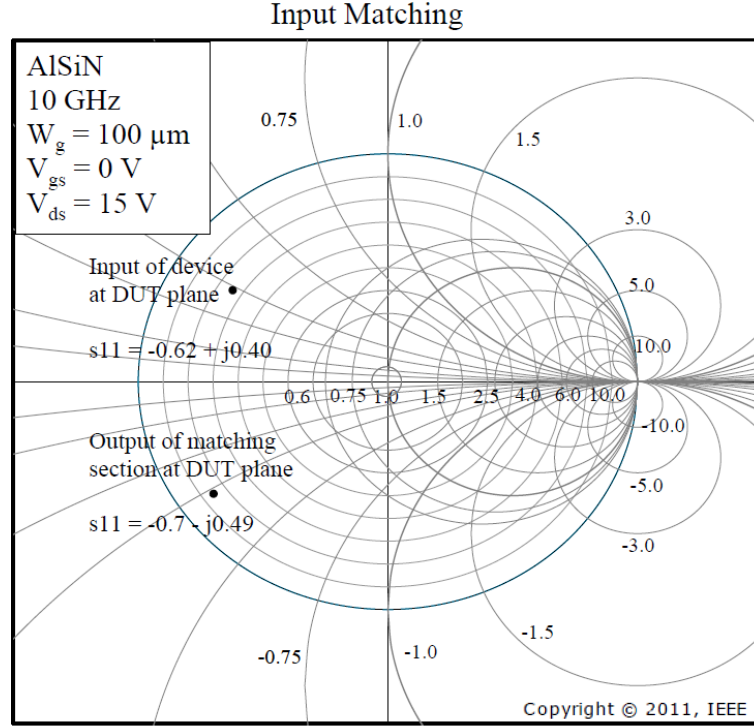


Figure 3.7:  $S_{11}$  parameter looking into the device input and looking back into the input tuning network with a  $100\ \mu\text{m}$  gate periphery,  $0.25\ \mu\text{m}$  gate length device.

A conjugate match at the output is measured in a similar fashion by breaking the connection at the output probe and measuring the  $s_{11}$  parameters looking into the output side of the device and the input side of output branch (Figure 3.8). Generally, however, the effectiveness of the match is most simply demonstrated by a power sweep (Figure 3.9). Since the matching is done at a fixed drive (fixed  $P_{in}$ ), we should expect that the match at that particular drive to be at its best. This is observed in the figure as a notable drop in reflected power at the tuning drive. The load impedance is usually set by the application, as the optimum tuning points for power, PAE, or gain may be different for the same device. The output tuner is scanned in the same manner as the input tuner, except the point of peak efficiency, gain, or output power is chosen instead of

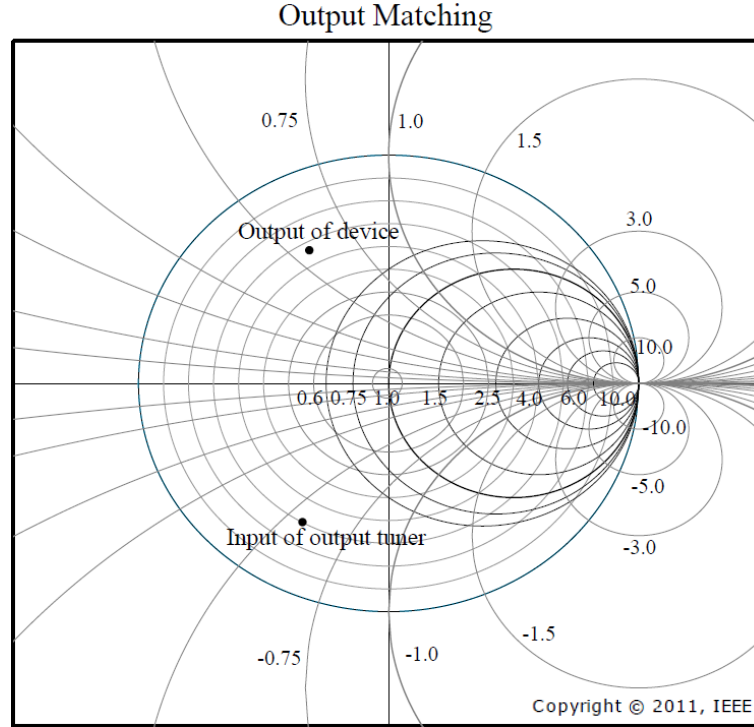


Figure 3.8:  $S_{11}$  parameter looking into the device output and into the output tuning network with a  $100\ \mu\text{m}$  gate periphery,  $0.25\ \mu\text{m}$  gate length device.

reflected power. Lastly, the load impedance of the second harmonic is set by scanning and optimizing the second harmonic tuner for whichever metric is chosen. The device and second harmonic branch  $s_{11}$  parameter are shown in Figure 3.10. Note that at the device plane, the second harmonic branch does not appear as a short. This is due to the fact that even though the tuner calibration at that point shows a short, when transformed through the intervening components (i.e diplexer, cables, and probes), the whole branch is not.

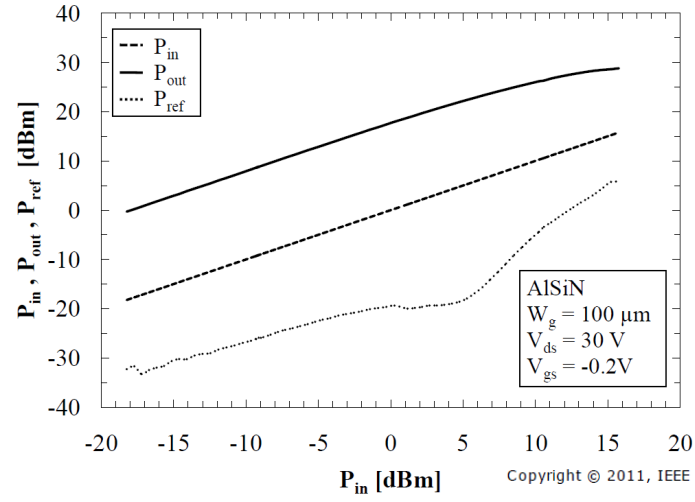


Figure 3.9: Input, output, and reflected power with drive.

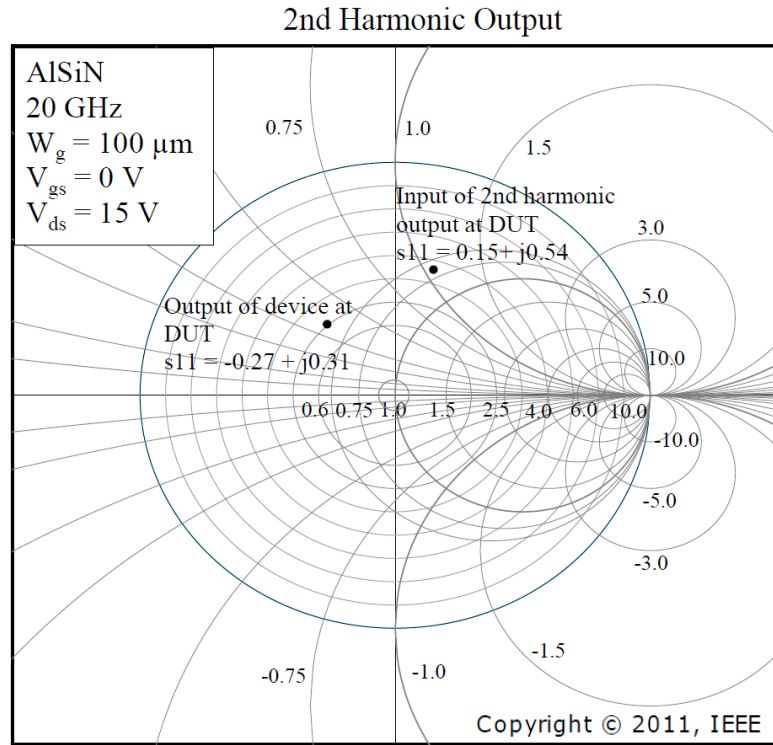


Figure 3.10:  $S_{11}$  parameter looking into the output of the device and into the second harmonic tuning network with a  $100 \mu\text{m}$  gate periphery,  $0.25 \mu\text{m}$  gate length device.



### 3.3.2 2nd harmonic termination

A significant second harmonic component at the output when the device was biased near pinch off allowed for study of the effects of harmonic loading. The theory of harmonic loading [59] has been studied in computer simulation [60] and demonstrated in many experiments. The effects of the higher order harmonics produced by the device have been documented both at the input [61] and output [62–67].

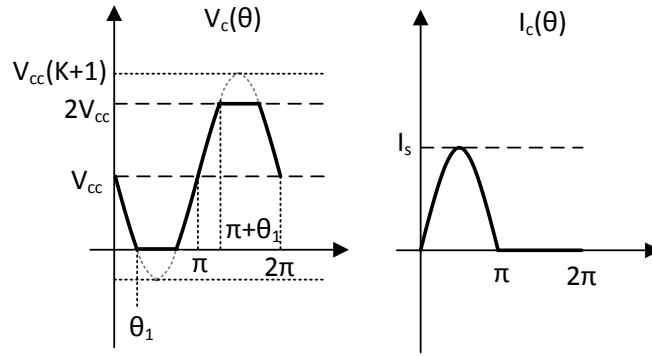


Figure 3.11: Voltage and current waveforms of an optimally driven Class B amplifier.

Second harmonic analysis is usually based on the theoretical optimally efficient class B amplifier. Snider [59] presented the optimal case through Fourier analysis. The current and voltage waveforms for the class B case are shown in Fig 3.11. Fourier analysis can be carried out on the collector (or drain) current. The expansion of  $I_c(\theta)$  gives the following coefficients:

Cosine:

$$I_{A0} = \frac{I_s}{\pi}$$

$$I_{A1} = 0$$

Sine:

$$I_{B1} = \frac{I_s}{2}$$

$$I_{Bn} = 0$$

$$I_{An} = \begin{cases} \frac{I_s}{\pi} \left( \frac{1}{1+n} + \frac{1}{1-n} \right) & n \text{ even} \\ 0 & n \text{ odd} \end{cases}$$

The expansion of  $V_c(\theta)$  gives:

Cosine:

Sine:

$$V_{A0} = V_{cc} \quad V_{B1} = V_{cc} \left[ \frac{2K\theta_1}{\pi} - \frac{K \sin(2\theta_1)}{\pi} + \frac{4 \cos(\theta_1)}{\pi} \right]$$

$$V_{An} = 0$$

$$V_{Bn} = \begin{cases} 0 & n \text{ even} \\ V_{cc} \left[ \frac{2K \sin(\theta_1 - n\theta_1)}{\pi} - \frac{2K \sin(\theta_1 + n\theta_1)}{\pi} + \frac{4 \cos(n\theta_1)}{\pi} \right] & n \text{ odd} \end{cases}$$

where  $K = \frac{1}{\sin(\theta_1)}$ .

As  $\theta_1$  goes to zero, the voltage waveform  $V_c(\theta)$  approaches a square wave, the collector (drain) efficiency approaches 100 %, and

$$I_{B1} = \frac{I_s}{2} \quad V_{B1} = \frac{4V_{cc}}{\pi}$$

Therefore, the power at the fundamental frequency is

$$P_{out}(\text{RF}) = \frac{V_{cc}I_s}{\pi}$$

The DC input is:

$$P_{in}(\text{DC}) = \frac{V_{cc}I_s}{\pi}$$

The impedances are therefore:

$$Z_1 = \frac{8 V_{cc}}{\pi I_s}$$

$$Z_n = \begin{cases} \frac{0}{I_{An}} = 0 & n \text{ even} \\ \frac{V_{Bn}}{0} = \infty & n \text{ odd} \end{cases}$$

Therefore, in order to achieve 100 % efficiency, even harmonics must be presented with zero impedance (a short) and odd harmonics must be presented with infinite impedance (open).

Theoretical analysis states that the power-added efficiency can be improved by 5-10 % by terminating the second harmonic in a short, which reflects the in-phase second harmonic power back to the device in the opposite phase, allowing it to contribute to the fundamental power [60]. Experiments on recent devices reflect this range, where improvements of PAE of 4.1 % [62] to as much as 10 % [66] have been reported.

The impact on efficiency has been of particular interest. In this work [58], the termination of the second harmonic was achieved using a two tuners, a fundamental and a second harmonic, both of which were adjusted to achieve maximum PAE. To study the effect of the second harmonic loading, a series of power sweeps were carried out at various tuner settings. First, it was confirmed that terminating the second harmonic in a short would maximize the output power and efficiency. When the tuner is “shorted”, the probe is all the

way down, or 0 mm “out”. The distance “out” increases as the probe is pulled out to approximate an open. Figure 3.12 shows the second harmonic power as a function of the tuner slide position with varying probe positions. When the probe is brought close to the transmission line—approximating a short—the second harmonic power is observed to have its largest swing in value over the range of the slide. Furthermore, it is observed (Figure 3.13) that when the second harmonic power is at a maximum, the first harmonic power is at a minimum, and vice versa. We may thus tune the second harmonic probe to get its maximum swing, and tune the second harmonic slide to catch the minimum value, thereby boosting the fundamental power.

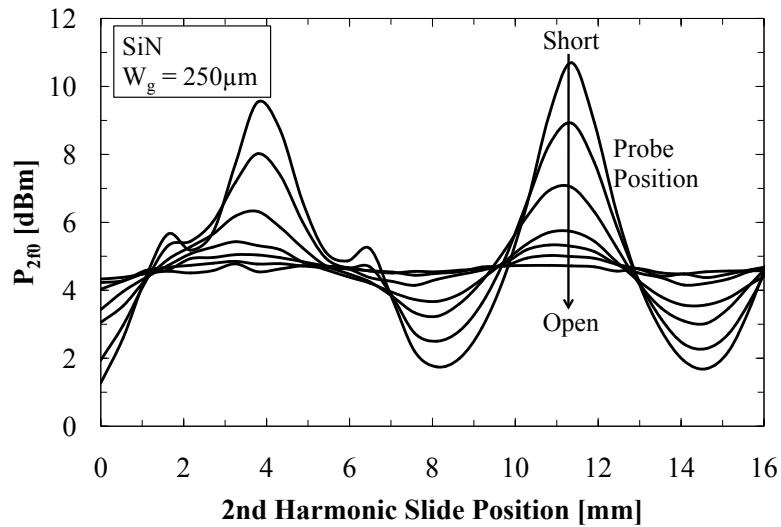


Figure 3.12: Second harmonic output power as a function of the second harmonic tuner slide and probe. The probe position ranged from 2.222 mm to 0.3175 mm out. The device was biased at  $V_{ds}^q = 15$  V,  $V_{gs}^q = -2.2$  V,  $I_d^q = 62.27$  mA.

Efficiency can also be increased from the theoretical maximum of 78.5 % of class B by operating the device in class C, where 100 % efficiency is possible. A study of the gate bias was done to observe the transition into class C operation, thereby boosting efficiency. The gate-source bias was swept from the quiescent

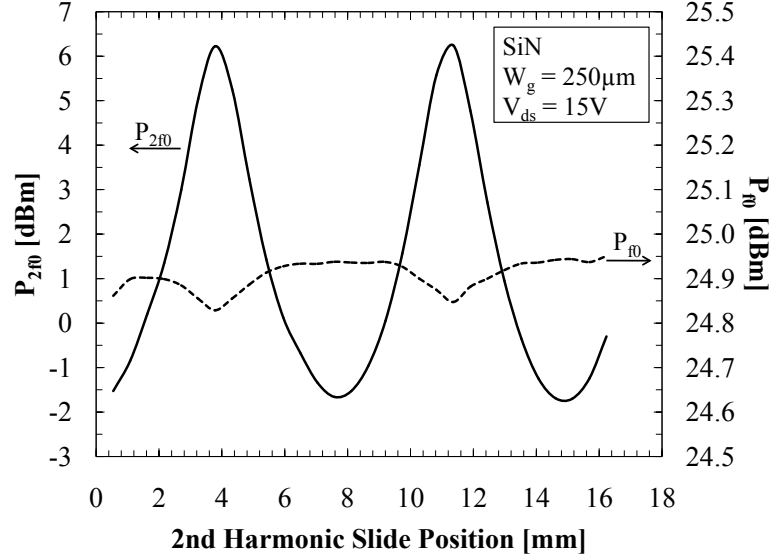


Figure 3.13: Second harmonic output power and fundamental power as a function of the second harmonic tuner slide. The second harmonic probe was fixed at 0.9525 mm out, and the device was biased at  $V_{ds}^q = 15$  V,  $V_{gs}^q = -2.2$  V,  $I_d^q = 62.27$  mA and driven at 11.54 dBm of input power.

voltage (the peak of transconductance) to close to pinch-off (Figure 3.14). For a 250  $\mu\text{m}$ , SiN-passivated device, the PAE increased from 63 % at  $V_{gs} = -2.2$  V to 70 % at  $V_{gs} = -3$  V.

## 3.4 Time Domain

### 3.4.1 Setup

A schematic of the time domain setup is shown in figure [switching bench]. The main difference between the load pull and time domain measurement setups is that the diplexer and second harmonic branch are removed, and the output is connected to an Agilent 71500A Microwave Transition analyzer. The calibration

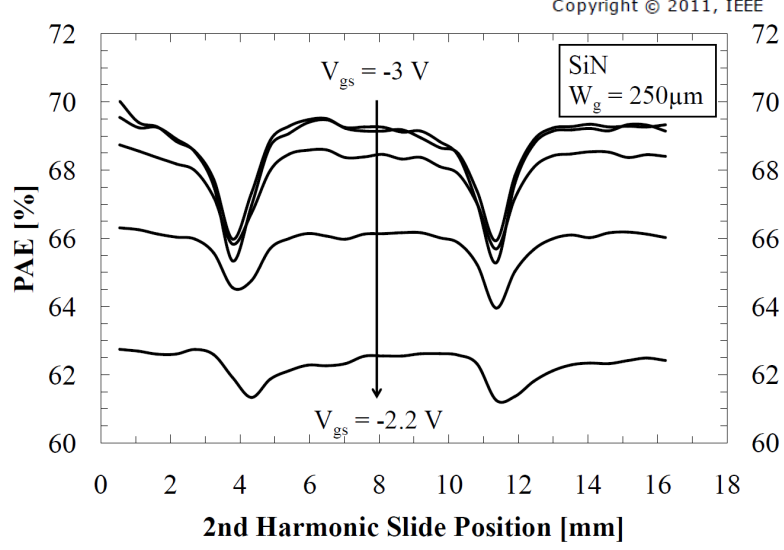


Figure 3.14: Power-added efficiency as a function of gate bias and second harmonic tuner slide position. The second harmonic probe was fixed at 0.635 mm out, and the device was biased at  $V_{ds}^q = 15 \text{ V}$ ,  $V_{gs}^q = -2.2 \text{ V}$ ,  $I_d^q = 62.27 \text{ mA}$  and driven at 11.54 dBm of input power.

of the time-domain setup is carried out in a similar fashion to that of the load pull setup, except that the calibration range encompasses the frequency range of the tuners, which is 1.8 to 18 GHz. A different, 20 dB, amplifier is used, as the frequency range of the more powerful amplifier is limited to a small region around 10 GHz. Typically, a 2.5 GHz signal is used to drive the device.

### 3.4.2 Transformation to the DUT Plane

A number of methods exist for shifting the reference plane from the MTA to the device under test (DUT). Historically, the shift in plane was done by transforming the measured voltage waveform through the measured S-parameters of the output branch [68]. This method relies on separately calculating the S-parameters of the branch at each harmonic frequency, and does not take into

account observed shifts in the frequency spectrum of the output signal. However, a more sophisticated method was developed by Green et al [69]. This method uses simple signal processing algorithms to transform the voltage and current waveforms. The method begins with the waveform measured by the MTA,  $v_{MTA}(t)$ . Its Fourier transform,  $V_{MTA}(f)$ , represents this signal in the frequency domain. The current waveform signal is therefore  $I_{MTA}(f) = V_{MTA}(f)/Z_0$ . The S-parameters of each piece of the output branch measured during calibration are cascaded, and the ABCD parameters are calculated for each tuner slide and probe setting at every frequency point through simple conversions [57]. The frequency-domain voltage and current waveforms are then determined by transforming the waveforms at the MTA through the ABCD parameters:

$$\begin{bmatrix} V_{DUT}(f) \\ I_{DUT}(f) \end{bmatrix} = \begin{bmatrix} A(f) & B(f) \\ C(f) & D(f) \end{bmatrix} \begin{bmatrix} V_{MTA}(f) \\ I_{MTA}(f) \end{bmatrix}$$

The sampled frequency domain waveforms are then converted back to the time domain by an inverse Fourier transform, and offset by the DC current and voltage to produce  $v_{DUT}(t)$  and  $i_{DUT}(t)$ . The RF loadline is then reconstructed from these waveforms. See Appendix A for details.

## CHAPTER 4

### MODELING

Device models are important and valuable tools in the design of discrete devices. First, representing a device as a network of lumped components is convenient for circuit design. Lumped element models are also easily scaled and are useful for predicting device performance with varying device geometry. Because the model elements are dependent on the physical structure of the discrete device, the model can also serve as an evaluation tool for layout design and process changes. For example, one might choose a certain geometry over another if one lowers the value of a parasitic capacitance in the model while the other does not. Or, if a critical resistance is found to be too high, the process may be changed to yield a thicker metal or a different structure might be used.

Models can also be used to predict device behavior in circuits by de-embedding the “intrinsic” device, separate from the pads and interconnects used to probe it. Furthermore, analyzing the effect changes in certain parameters have on the theoretical performance of the device allows for targeted changes in layout and fabrication to address problems or enhance positive effects.

#### 4.1 Small Signal Model

The methodology used for small-signal parameter extraction described in this section was described by Shealy et al [70], and is based on the Dambrine model [71]. Certain modifications were made to account for the structure of the coplanar waveguide probe pads, which create shunt capacitive parasitics, as well



as series inductances and resistances at each device terminal. Some models have included capacitive parasitics from the asymmetric CPW produced by the source, gate, and drain metals on the active device mesa [72], and these have been included in this model as well. These are referred to as “on-mesa” capacitances. However, instead of treating them as distinct elements which require high frequency validation, it was found that these “on-mesa” or “interconnect” capacitances can simply be lumped into the extrinsic pad capacitances with little error, thus reducing the complexity of the model [70]. Similar models have been used to successfully model coplanar probed GaAs pHEMTs [73,74]. This also considers the effects of gate leakage and measurement-based corrections are made to the intrinsic device.

The lumped element model is shown in Figure 4.1. At the center is the conventional, intrinsic, high frequency FET. This consists of the voltage-dependent current source defined by the gate-source voltage  $V^1$ , the gate/drain delay  $\tau$ , and intrinsic RF transconductance  $g_{m0}$  as:

$$I_{gm} = g_{m0} \exp(-j\omega\tau) V^1$$

The other intrinsic elements include the gate-source, gate-drain, and drain-source capacitances (denoted by  $C_{gs}$ ,  $C_{gd}$ , and  $C_{ds}$ ), the gate-source and gate-drain resistances (denoted by  $R_{gs}$  and  $R_{gd}$ , and the output conductance  $G_{ds}$ . There are also two conductive shunts,  $G_{gs}$  and  $G_{gd}$ , which are determined by the transfer curve measurement:

$$G_{gs} = \frac{I_{g,max}}{V_g(I_{g,max})} \quad G_{gd} = G_{gs} \cdot \alpha_{gd}$$

The term  $\alpha_{gd}$  is a fitting factor used to optimize low frequency matching, and was determined to be approximately 10.

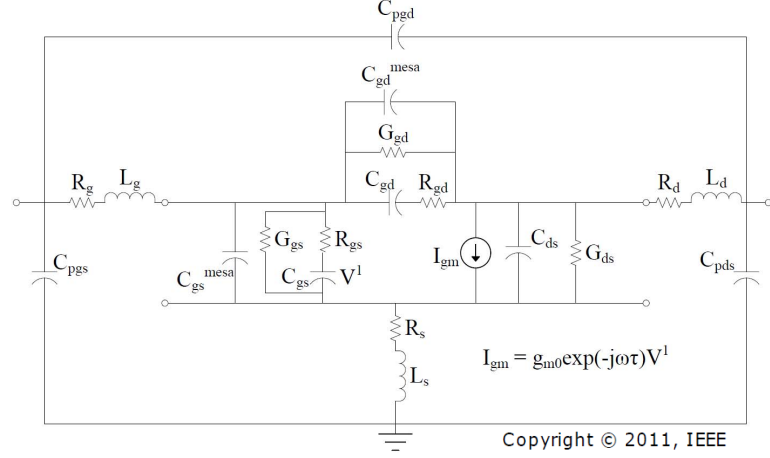


Figure 4.1: Circuit model

The extrinsic elements include the gain-source, gate-drain, and drain-source pad capacitances ( $C_{pgs}$ ,  $C_{pgd}$ , and  $C_{pds}$ ), and the series resistance/inductance pairs  $R_s/L_s$ ,  $R_g/L_g$ , and  $R_d/L_d$ .

#### 4.1.1 Parameter Extraction

##### Pad Capacitance

The first step in the parameter extraction is the determination of the pad capacitances. This is done under “cold-FET” conditions, in the regions where the capacitances are bias-independent [70]. For  $C_{pds}$  and  $C_{pgs}$  the gate is biased beyond pinch-off to deplete the channel and the drain is biased at 0 V, thereby effectively removing the intrinsic portion of the device by making it an open circuit. Since there is no current, the effect of the series parasitics may be ig-

nored at low frequency. For  $C_{pgd}$ , the drain is positively biased at 15 V to fully deplete the gate-drain region. Because this leaves a simple  $\pi$  capacitor network, Y-parameters are the natural choice [75]. The device Y-parameters are measured, and the pad capacitances are calculated:

$$\begin{aligned} C_{pgs} &= \frac{\Im(Y_{11})}{\omega} + \frac{\Im(Y_{12})}{\omega} \\ C_{pds} &= \frac{\Im(Y_{22})}{\omega} + \frac{\Im(Y_{12})}{\omega} \\ C_{pgd} &= \frac{-\Im(Y_{12})}{\omega} \end{aligned}$$

The lowest frequency value of each is chosen.

### Series Parasitics

In order to find the iseries parasitics, the intrinsic device must be biased so as to approximate a short. However, there will still be a gatesource intrinsic capacitance ( $C_{gs}^s$ ) that cannot be ignored, because doing so will lead to a negative gate inductance [70].

This capacitance is derived from the  $p^+n$  short-base diode forward bias diffusion capacitance:

$$\frac{C}{I} = \frac{W_n^2}{2 \left( \frac{kT}{q} \right)^2 \mu_p}$$

Setting the diffusion distance to the sum of the barrier thickness  $t_{AlGaN}$  and debye length  $\lambda_D$  to get:

$$\frac{C_{gs}^s}{I_g} = \frac{(t_{AlGaIn} + \lambda_D)^2}{2\mu_n \left(\frac{kT}{q}\right)^2}$$

The gate bias is set by having the drain at 0 V and the gate has a constant current, which scales with periphery ( $I_g = W_g \times 50$ ). The break frequency of the parallel combination of the diffusion capacitance and the gate dynamic resistance is around 6 GHz, but as the parasitic extraction is done at high frequency (50 GHz), the dynamic resistance can be ignored as the diffusion capacitance effectively shorts it. The gate inductance still needs to be corrected, however, due to the capacitive load of the intrinsic device.

The extraction is done by measuring the Y-parameters, denoted as  $Y_{xx}$  below, and subtracting the pad capacitances to get the corrected Y's,  $Y_{xxc}$ .

$$Y_{11c} = Y_{11} - \Im(j\omega(C_{pgd} + C_{pgs}))$$

$$Y_{12c} = Y_{12} - \Im(-j\omega C_{pgd})$$

$$Y_{21c} = Y_{21} - \Im(j\omega C_{pgd})$$

$$Y_{22c} = Y_{22} - \Im(j\omega(C_{pgd} + C_{pds}))$$

These corrected Y-parameters are then converted to Z-parameters, and the series parasitics are then calculated, including the correction to the gate inductance.

$$R_s = \Re(Z_{12c}) \quad R_g = \Re(Z_{12c} - R_s) \quad R_d = \Re(Z_{22c} - R_s)$$

$$L_s = \frac{\Im(Z_{12c})}{\omega} \quad L_g = \frac{\Im(Z_{11c})}{\omega} - L_s + \frac{1}{\omega^2 C_{gs}^s} \quad L_d = \frac{\Im(Z_{22c})}{\omega} - L_s$$

### Intrinsic Device Parameters

Once all the extrinsic parasitics are known, the device can be measured at the desired operating point. This is when the gate is biased at  $V_{gs}^q$ , as determined in section 3.1.1 from the peak of the transconductance plot, and the drain at 15 V.

First, the Y-parameters are measured, and the pad capacitances are subtracted, as for the series parasitic extraction. These corrected Y-parameters ( $Y_{xxc}$ ) are then converted to Z-parameters ( $Z_{xxc}$ ), and the series parasitics are subtracted to get the intrinsic Z-parameters ( $Z_{xxi}$ ):

$$\begin{aligned} Z_{11i} &= Z_{11c} - j\omega(L_g + L_s) - R_g - R_s & Z_{12i} &= Z_{12c} - R_s - j\omega L_s \\ Z_{21i} &= Z_{21c} - R_s - j\omega L_s & Z_{22i} &= Z_{22c} - j\omega(L_s + L_d) - R_d - R_s \end{aligned}$$

These are then converted to Y-parameters ( $Y_{xxi}$ ), and the intrinsic parameters are calculated:

$$\begin{aligned} C_{gs} &= \frac{\Im(Y_{11i} + Y_{12i})}{\omega} & C_{ds} &= \frac{\Im(Y_{22i} + Y_{12i})}{\omega} & C_{gd} &= \frac{-\Im(Y_{12i})}{\omega} \\ R_{gs} &= \frac{\Re(Y_{11i} + Y_{12i}) - G_{gs}}{(\omega C_{gs})^2} & R_{gd} &= \frac{\Re(-Y_{12i}) - G_{gd}}{(\omega C_{gd})^2} & G_{ds} &= \Re(Y_{22i} + Y_{12i}) \end{aligned}$$

$$g_{m0} = |Y_{21i} - Y_{12i}| |1 + j\omega C_{gs} R_{gs}| \quad \tau = -\frac{\angle((Y_{21i} - Y_{12i})(1 + j\omega C_{gs} R_{gs}))}{\omega}$$

## 4.2 Extrinsic Parameter Effects

After all parasitic and intrinsic device parameters have been determined, the intrinsic  $f_T$  and  $f_{\max}$  can be calculated by constructing the S-parameters from the intrinsic portion of the network. The extrinsic  $f_T$  and  $f_{\max}$  can also be modeled by simply adding the extrinsic parasitic elements. Because the model is built on the individual lumped elements, we can easily analyze the effect changing the value of any one parameter can have on the device metrics.

In order to simulate the relative effects of individual parasitic elements, the value of the element was swept from zero to its extracted value and the intrinsic device simulation was run at each step. It was found that the gate-drain pad capacitance has a significant effect on both the  $f_T$  and  $f_{\max}$ . The  $f_T$  is also strongly affected by the gate-source pad capacitance and source resistance, though as periphery increases, the gate-source capacitance has an increasingly dominant effect. For example, an  $f_T$  of 66 GHz was extracted for an AlSiN-passivated device with gate length of 0.15  $\mu\text{m}$  and periphery of 100  $\mu\text{m}$ . The results of the elimination of the gate-drain and gate-source pad capacitances and the series parasitic resistances is shown in Figure 4.2. The lines labeled “Extrinsic” and “Intrinsic” indicate the simulated value of  $f_T$  from the entire model, including all parasitics, and from just the intrinsic portion, respectively. For each parasitic, the bar shows the value of  $f_T$  that the model predicts when that parasitic is eliminated.

The  $f_T$  was simulated to increase to 83 GHz by zeroing the gate-drain pad capacitance alone, and increase to 91 GHz by zeroing the gate-source pad capacitance alone. The source resistance was also investigated as it has known effects on  $f_T$  [76]. Zeroing the source resistance alone increased the  $f_T$  to 74.5 GHz.

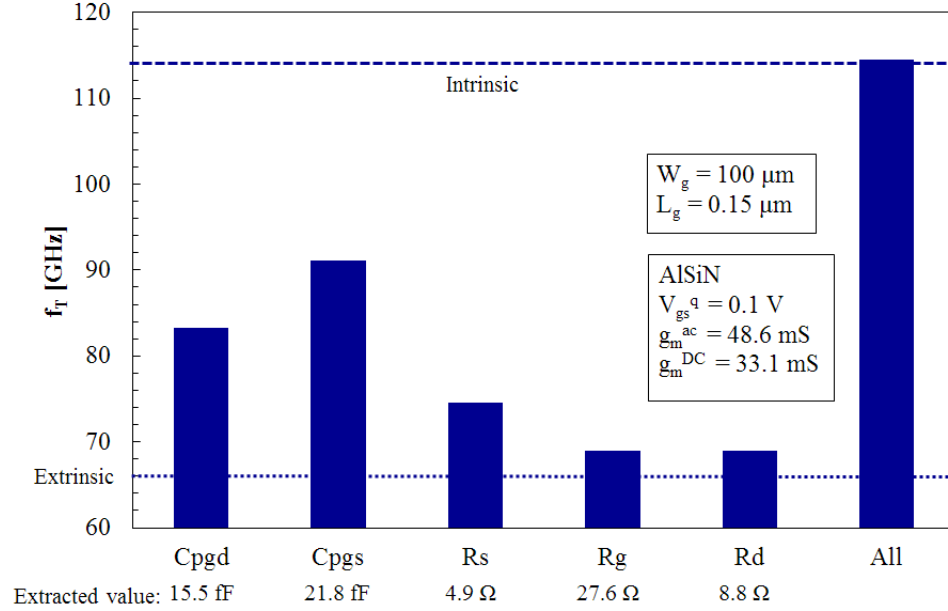


Figure 4.2: Prediction of the value of  $f_T$  attainable by removing certain parasitic elements of at  $0.15 \times 100 \mu\text{m}$  device. The values of the extracted parasitics are also shown.

For a  $0.15 \mu\text{m}$  gate length,  $250 \mu\text{m}$  periphery device, the  $f_T$  increased from 69 GHz to 102 GHz with the removal of the gate-drain pad capacitance alone, and 136 GHz with the removal of the gate-source pad capacitance alone (see Figure 4.3). Zeroing the source resistance alone increased the  $f_T$  to 93 GHz.

The  $f_{\text{max}}$  is affected by the output conductance and for smaller peripheries, the gate-drain pad capacitance dominates the decrease in  $f_{\text{max}}$ , but the effects of the gate resistance and output conductance increase with increasing gate pe-

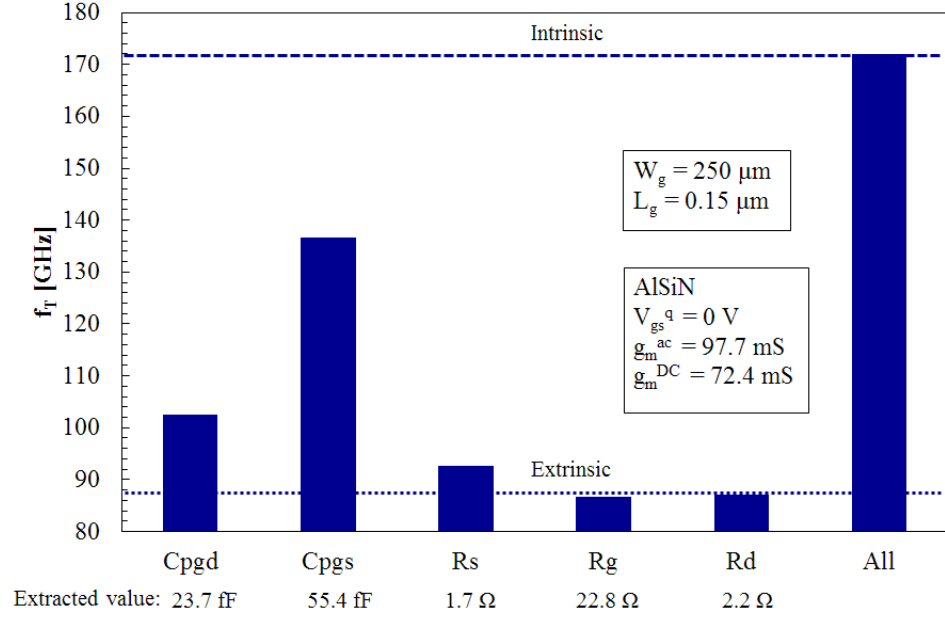


Figure 4.3: Prediction of the value of  $f_T$  attainable by removing certain parasitic elements of at  $0.15 \times 250 \mu\text{m}$  device. The values of the extracted parasitics are also shown.

riphery. A  $0.25 \mu\text{m}$  gate length,  $100 \mu\text{m}$  periphery device, the extracted  $f_{\text{max}}$  of 125 GHz increased to 262 GHz with the elimination of the gate-drain pad capacitance, but just 136 GHz with the elimination of the gate resistance, and saw no change with the elimination of the output conductance (Figure 4.4).

However, a  $250 \mu\text{m}$  periphery device saw an increase in  $f_{\text{max}}$  from 66 GHz to 87 GHz without the gate-drain pad capacitance, 80 GHz without the gate resistance, and 86.6 GHz without the output conductance (Figure 4.5).

#### 4.2.1 Gate Inductance

When the metrics ( $f_T$ ,  $f_{\text{max}}$ ) were plotted versus the value of a parasitic, the curves were generally monotonically decreasing with increasing parasitic value.



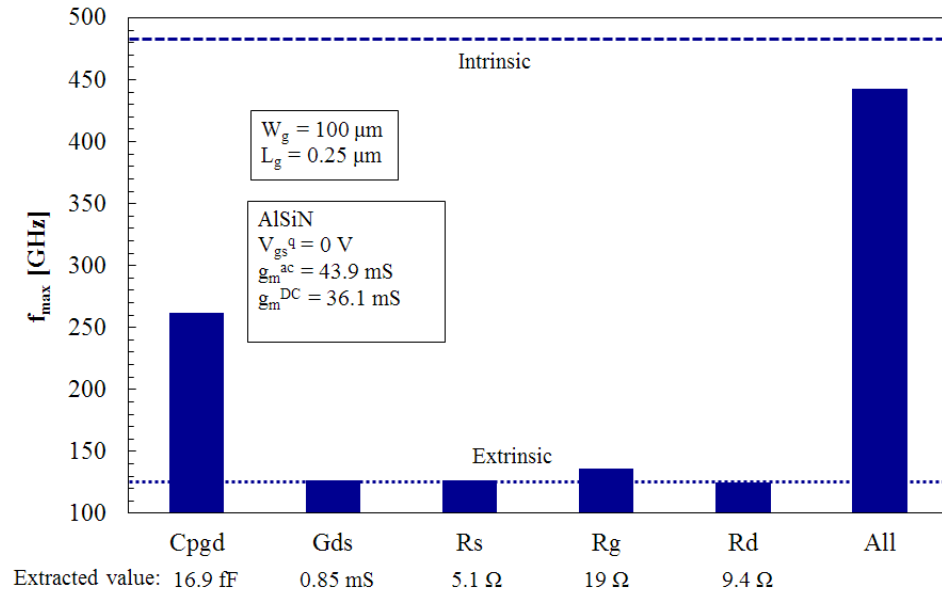


Figure 4.4: Prediction of the value of  $f_{\max}$  attainable by removing certain parasitic elements of at  $0.15 \times 100 \mu\text{m}$  device. The values of the extracted parasitics are also shown.

An exception was found with the gate inductance.

A  $0.25 \times 100 \mu\text{m}$  device was used for these simulations. The as-extracted gate inductance was 55.2 pH. A series of simulations were performed with the gate inductance increasing from 200 to 1700 pH in steps of 300 pH. As gate inductance increased, a peak was observed in the plot of  $|h_{21}|$  (Figure 4.6) and a double peak in plot of MSG/MAG (Figure 4.7).

The peaks became greater in magnitude and shifted to lower and lower frequencies as the gate inductance was increased. These peaks suggest that a resonance is occurring at those values of gate inductance. While eventually the increasing inductance forces the  $f_T$  and  $f_{\max}$  to degrade, the boost in gain at lower frequency is useful. In fact, an interstage matching inductor is used in Low Noise Amplifiers to improve power transfer to the gate and reduce noise [77].

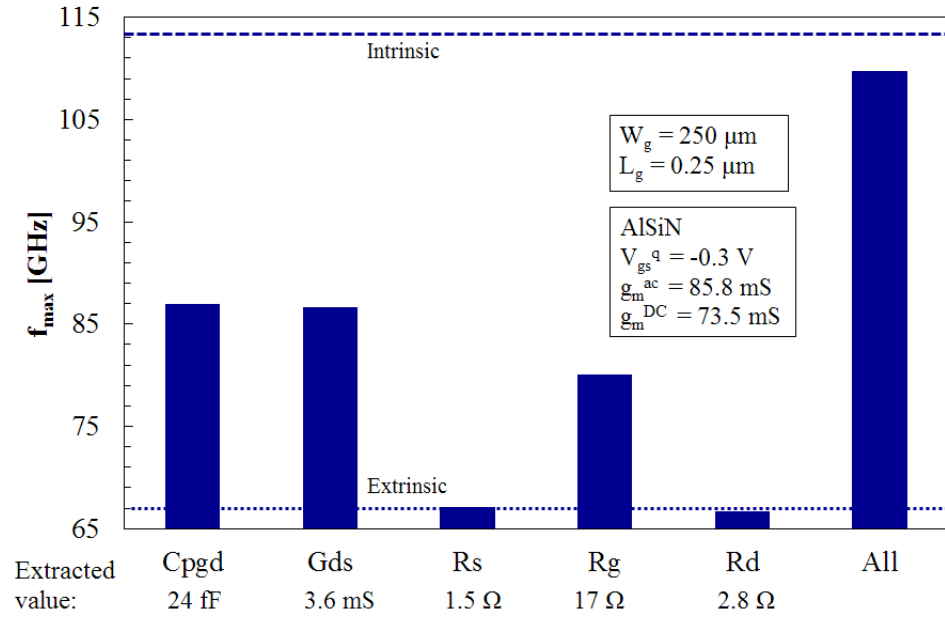


Figure 4.5: Prediction of the value of  $f_{\max}$  attainable by removing certain parasitic elements of at  $0.15 \times 250 \mu\text{m}$  device. The values of the extracted parasitics are also shown.

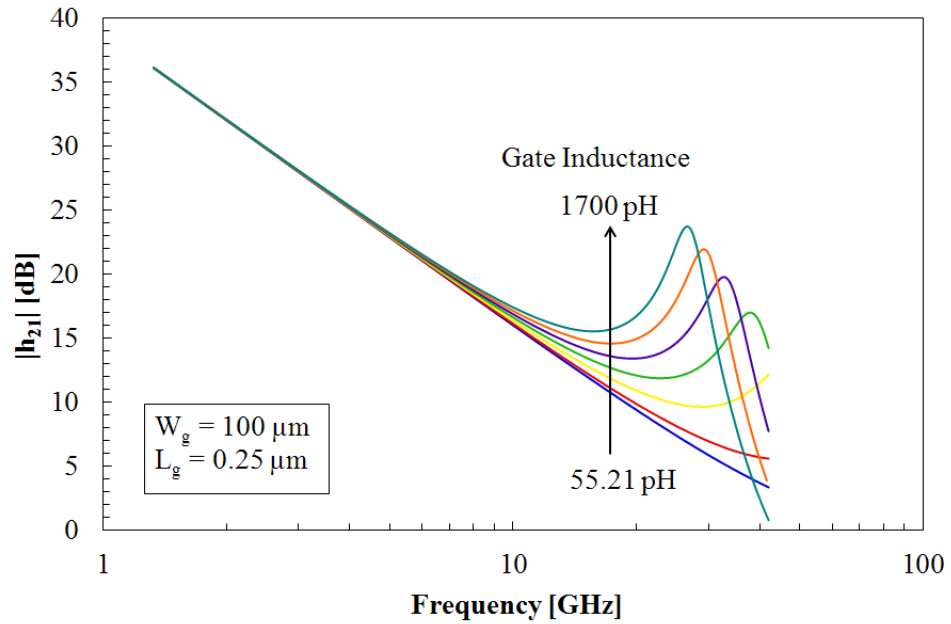


Figure 4.6: Simulation of the magnitude of the hybrid parameter  $h_{21}$ . As the gate inductance increases, the observed peak shifts to lower frequency.

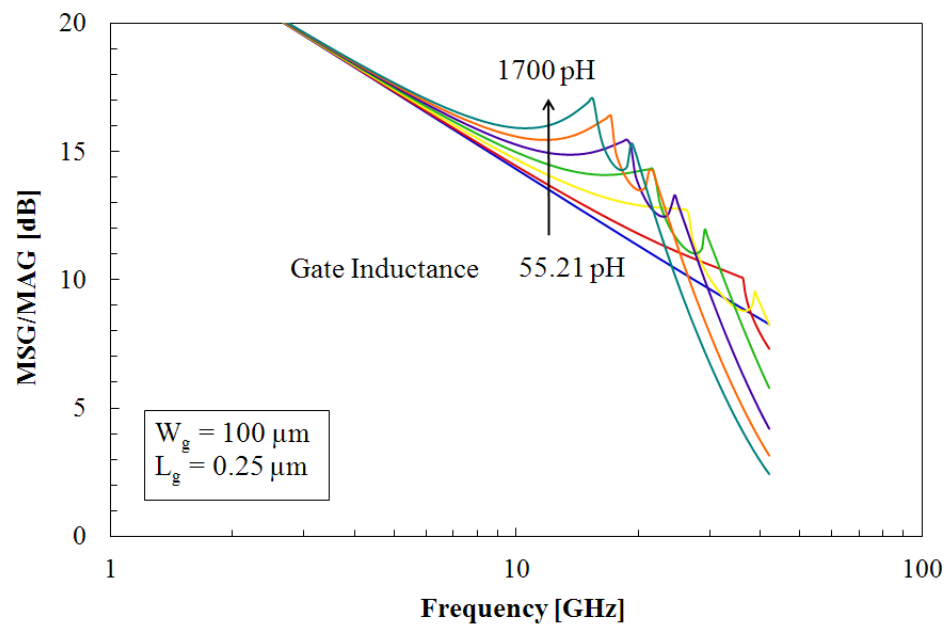


Figure 4.7: Simulation of the maximum gain with increasing gate inductance.

## CHAPTER 5

### PASSIVATION STUDY

#### 5.1 Motivation

Device performance is fundamentally rooted in the quality of the material in both the epitaxial layers and at the surface. The quality of the epitaxial layers has improved with more sophisticated growth methods, such as AlN spacer layers and buffers, reducing the number of dislocations and alloy related scattering [78]. However, even in the best material, surface trapping effects will invariably be observed and are considered unavoidable due to the polarization of the material.

Vetury et al first measured the effects of surface states by using floating gates as potential probes to measure the surface along the gate-drain access region [79]. An extension of the gate-drain depletion region was observed that did not correspond to the ionized donor density, which indicated the presence of an additional negative charge at the surface. This model of a “virtual gate” was later supported by deep level transient spectroscopy [80].

This additional charge is introduced by electrons injected by the gate entering trapping states at the surface. These traps are thought to result from dangling bonds at the surface, threading dislocations, and ions absorbed into the bare surface from the environment. When the states become occupied, a layer of charge forms at the surface, depleting the channel in the gate-drain region. It is estimated that the time constants of these trapping states range from microseconds to seconds. Therefore, it is not possible to fully modulate the chan-

nel during RF operation, which results in reduced RF current swing and output power [81], and gate and drain lag [82]. This phenomenon has been referred to as current degradation, slump, and dispersion. Furthermore, conduction and ionization along this charged layer is thought to contribute to lower breakdown voltages [81].

The solution to alleviating trapping and dispersion is surface passivation, which has been shown to reduce surface trapping and dispersion in the channel. The exact mechanism for how passivation reduces the density of trapping states is under debate. Still, the use of thin passivation layers such as SiN have shown marked improvement in RF power, efficiency, and breakdown voltage, as well as improve DC characteristics such as current and alleviate gate lag [81, 83–86].

Finally, passivation has also been shown to increase the concentration of the 2DEG in the channel [4]. In Section 2.1.3, the sheet charge density was given as:

$$n_s = \frac{1}{q} \frac{\sigma^{\text{AlGaIn/GaN}} - c_{\text{AlGaIn}}(\phi_b - \Delta E_c) - c_{\text{GaIn}}\phi}{1 + c_{\text{AlGaIn}} \frac{\pi \hbar^2}{q^2 m^*}}$$

Similarly, the sheet charge density in the channel for a passivated structure (see Figure 5.1) can be derived by applying Gauss' law [4]:

$$a_{in}E_{in} + a_1E_1 = -\phi_B + \Delta E_c^{in} + \Delta E_c - \Delta$$

where  $a_{in}$  is the thickness of the passivation layer,  $E_{in}$  is the electric field across the dielectric,  $\Delta E_c^{in}$  is the conduction band offset between the passivation and the AlGaIn, and  $\phi_B$  is the surface potential on the passivation. With  $\sigma_T$  representing the positive charge trapped at the passivation/AlGaIn interface,  $c_B$  is the series combination of the passivation and AlGaIn capacitance, and  $\Psi_P = \phi_B - \Delta E_c^{in} - \Delta E_c$ ,

the induced sheet density is then:

$$n_s = \frac{1}{q} \frac{\sigma^{\text{AlGaIn/GaN}} - c_B \Psi_P - c_{\text{GaN}} \phi - \frac{c_B}{c_{in}} (\sigma^{\text{AlGaIn}} - \sigma_T)}{1 + c_B \frac{\pi \hbar^2}{q^2 m^*}}$$

This model predicts that if  $\sigma_T = \sigma^{\text{AlGaIn}}$  (the interface is neutral), the extra term drops out, and leaves simply the same equation with as the unpassivated case, only with the series combination of capacitances. This would mean that any thickness passivation layer would actually *increase* the 2DEG concentration in the channel. This assertion was confirmed by Hall measurements.

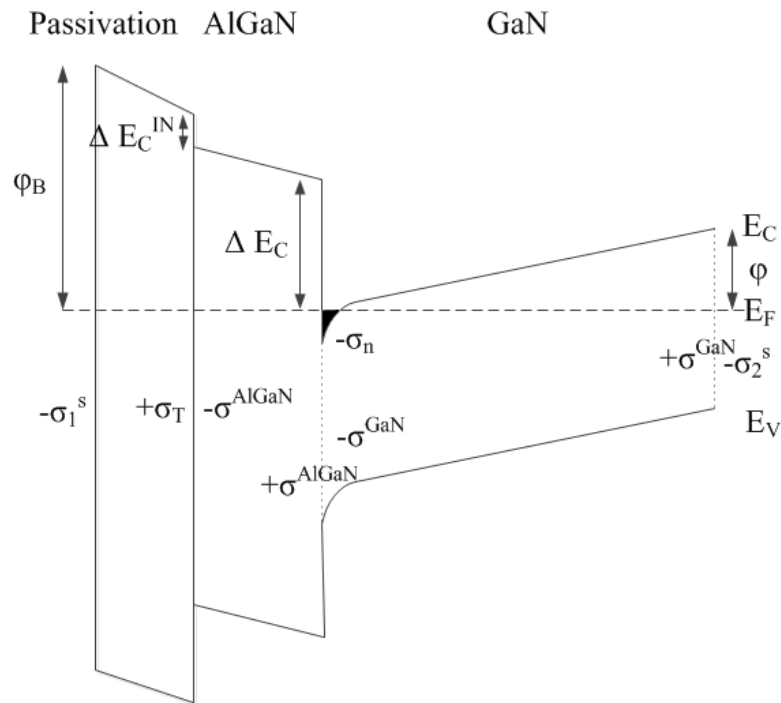


Figure 5.1: Band diagram of a passivated AlGaIn/GaN heterojunction, after Prunty et al [4].

Despite its many positive effects, there is one slight drawback to passivation, and that is that the passivation layer increases the gate-source capacitance (a key parasitic), and creates a resistive shunt in both the gate-source and gate-drain circuits. A dielectric that adequately passivates the surface without cre-

ating large parasitic resistances and capacitances would be ideal. To this end, a comparison between two passivation materials, SiN and AlSiN, on side-by-side fabricated devices was performed. Each dielectric was deposited by a high temperature LPCVD process to a thickness of roughly 30 nm producing low defect, hydrogen-free (relative to more common methods) films. AlSiN was used due to its larger bandgap and its expected lower permittivity at microwave frequencies.

## 5.2 Fabrication

AlSiN and SiN films were deposited in a modified low-pressure chemical vapor deposition (LPCVD) system onto etched mesa-isolated AlGa<sub>0.25</sub>N/GaN HEMT structures with 25 nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barriers grown on semi-insulating SiC. Dielectric deposition was performed at 750 °C at a pressure of 2 Torr with Trimethylaluminum, Dichlorosilane, and Ammonia as precursors. The conditions for deposition of the SiN films were adjusted to produce low stress, slightly Si rich films. The Aluminum fraction was controlled by the Trimethylaluminum flux, and was measured to be approximately 6 atomic percent by X-Ray Photoelectron Spectroscopy. At a wavelength of 1  $\mu\text{m}$ , the refractive index was measured to be 2.008 for AlSiN, and 2.014 for SiN. A side-by-side CV comparison measurement provided a 2DEG concentration of  $7.5 \times 10^{12} \text{ cm}^{-2}$  in an unpassivated sample,  $8.9 \times 10^{12} \text{ cm}^{-2}$  in a SiN-passivated sample, and  $7.1 \times 10^{12} \text{ cm}^{-2}$  in an AlSiN-passivated sample. SiN-passivated structures had a corresponding sheet resistance of approximately 450  $\Omega/\text{square}$ . Ta/Ti/Al/Mo/Au source/drain, and Ni/Au gate contacts were evaporated on windows through the dielectric etched using CF<sub>4</sub>, and SF<sub>6</sub>/BCl<sub>3</sub>/Ar RIE etches, respectively, de-

finned by electron beam lithography. A cross-sectional diagram of the HEMT structure is shown in Figure 5.2.

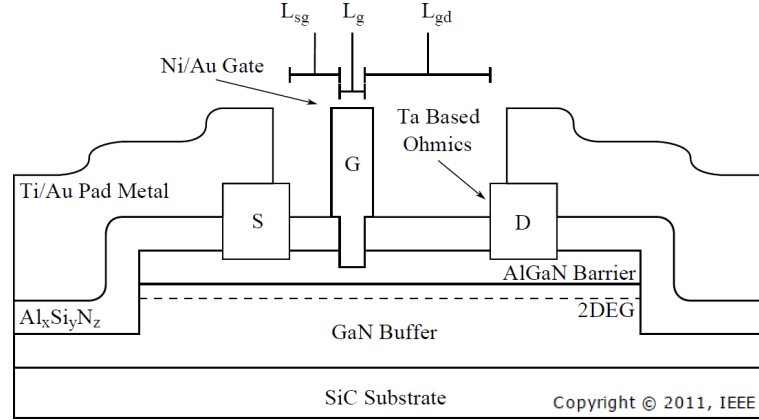


Figure 5.2: Cross-sectional schematic of HEMT structure, showing design parameters.

### 5.3 Small Signal Comparison

After fabrication, the 100  $\mu\text{m}$ , 250  $\mu\text{m}$ , and 400  $\mu\text{m}$  total gate periphery, dual-gate “U”-layout devices were characterized on-wafer using coplanar waveguide probes contacting Ti/Au probe pads. DC and small signal measurements were taken, as well as large signal measurements on a 10 GHz CW harmonic load-pull system.

The small signal device parameter extraction measurements were taken using an HP 8510C, 50 GHz network analyzer, with DC bias supplied by an Agilent 4142B connected to the network analyzer bias tees. The combination of probes, cables, and connectors was calibrated from 500 MHz to 42 GHz using a co-planar impedance standard substrate [87].



### 5.3.1 DC Results

The pinch-off voltages of the SiN and AlSiN-passivated devices were approximately -2.5 and -1.5 V, respectively, while the as-grown pinch-off was -4 V. This indicates that the barrier layers were recessed by the gate window etch by differing amounts. Figure 5.3 shows the pinch-off voltages measured for both types of passivation as a function of gate length. The quiescent voltage was chosen as the point of maximum transconductance for all devices. The DC-IV output curves for two 250  $\mu\text{m}$  periphery, 0.15  $\mu\text{m}$  gate length devices are shown in Figure 5.4. With the gate forward biased at 2 V, the AlSiN-passivated device had a knee voltage of 3.4 V, while the SiN-passivated device had a knee voltage of 2.8 V. The AlSiN devices also showed an order of magnitude lower gate leakage, as seen in Figure 5.5.

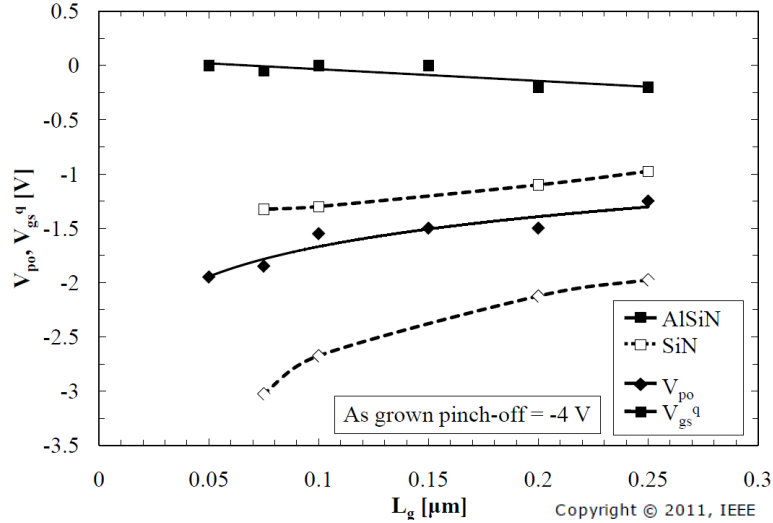


Figure 5.3: Pinch-off and quiescent voltages of AlSiN and SiN passivated devices

The maximum drain current at  $V_g = 2$  V and  $V_d = 10$  V was 209 mA for the AlSiN-passivated device and 218 mA for the SiN-passivated device. The inverse

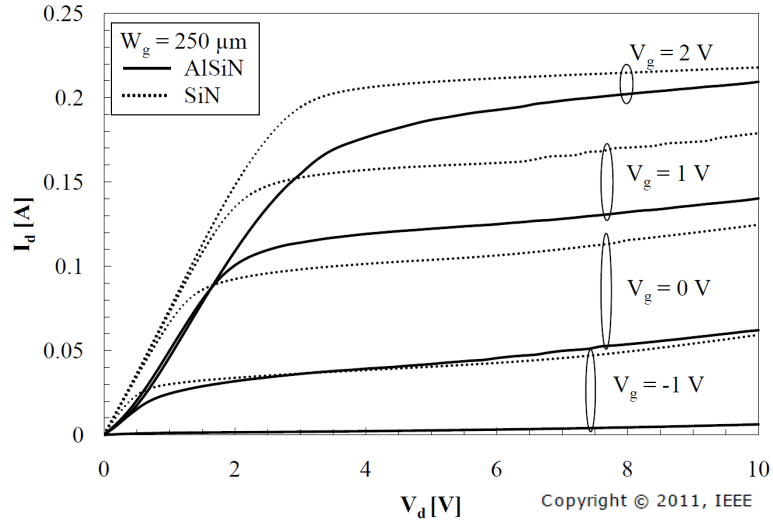


Figure 5.4: DC drain current for two  $0.15\ \mu\text{m}$  gate length,  $250\ \mu\text{m}$  periphery devices.

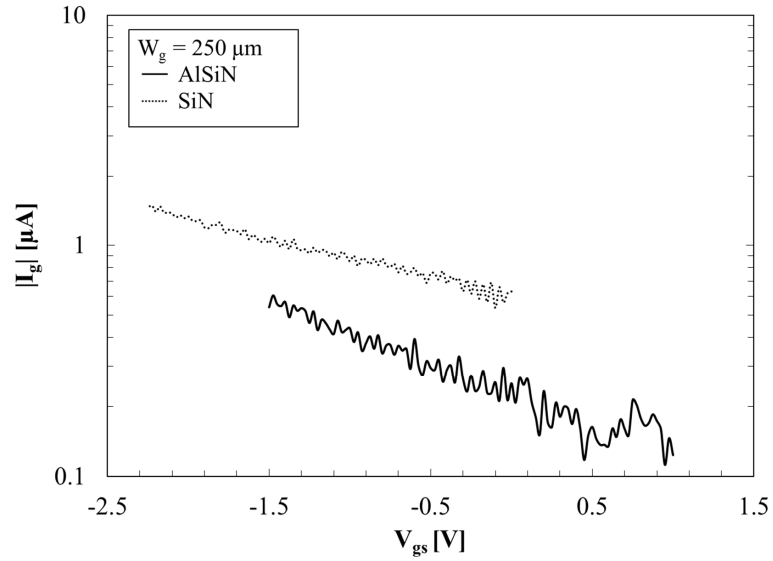


Figure 5.5: DC gate current for two  $0.15\ \mu\text{m}$  gate length,  $250\ \mu\text{m}$  periphery devices.

of the drain current with respect to drain voltage is also shown in Figure 5.6. The upturn at low drain bias visible for the AlSiN-passivated device corresponds to the measured increase in access resistance.

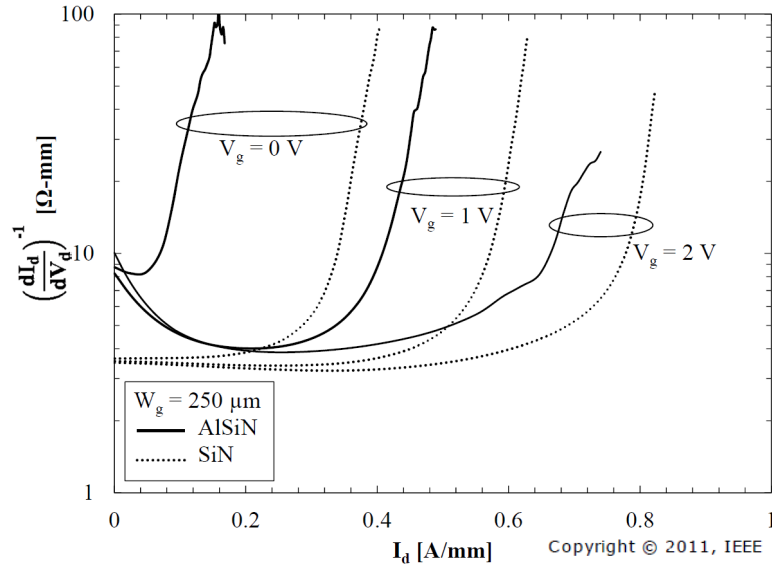


Figure 5.6: Inverse of the derivative of the drain current with respect to drain voltage for two  $0.15\mu\text{m}$  gate length,  $250\mu\text{m}$  periphery devices.

### 5.3.2 Small Signal Results

Parameter values obtained using small signal model extraction as described by Shealy et al [70], as based on the Tasker and Hughes model [73] and described in Section 4.1. The parasitic elements were extracted by biasing the devices at two operational extremes, approximating either a short or open circuit, which allows for the extraction of capacitive and inductive elements. The extraction was carried out over a range of biases, and the values in the bias-independent regions were used.

Devices with both types of passivation showed trends similar to previous work [70]. For both passivation schemes, small periphery devices exhibited lower parasitic capacitances, but higher series parasitic resistances. Gate resistance scaled inversely with gate length.

Several significant differences in the small signal performance of the two dielectrics were observed. In particular, lower values for several key parasitics were observed for the AlSiN-passivated devices.

The access (source and drain) resistances were found to be comparable for both AlSiN- and SiN-passivated devices under standard extraction conditions. To observe the changes in access resistance with drain current, the gate voltage was swept from pinch-off into forward bias and the resistance values were extracted at each point. For both SiN and AlSiN, the drain resistance was bias-independent. However, the source resistance was found to increase non-linearly with drain current in the SiN-passivated devices. This effect is attributed to large longitudinal electric fields in the source-gate region [88]. As shown in Figure 5.7, the AlSiN-passivated devices did not exhibit this behavior, as both the source and drain resistances remained relatively bias-independent.

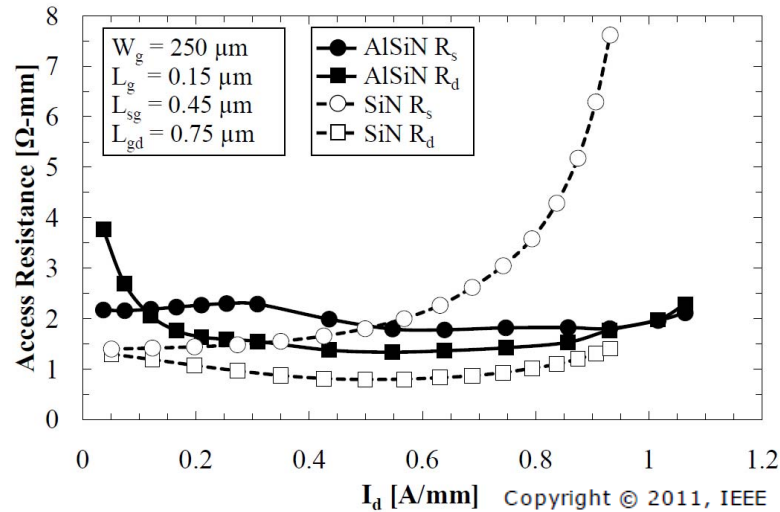


Figure 5.7: Behavior of extracted access resistance as a function of drain current for devices of both passivation schemes. The SiN-passivated devices exhibit significant non-linearity at high drain currents.

Another set of key parasitics that showed significant differences between

the two passivation materials was the pad capacitance. Figure 5.8 shows the gate-drain pad capacitance for various periphery devices. The increase with periphery is due to the physically larger structure of the metal pads.

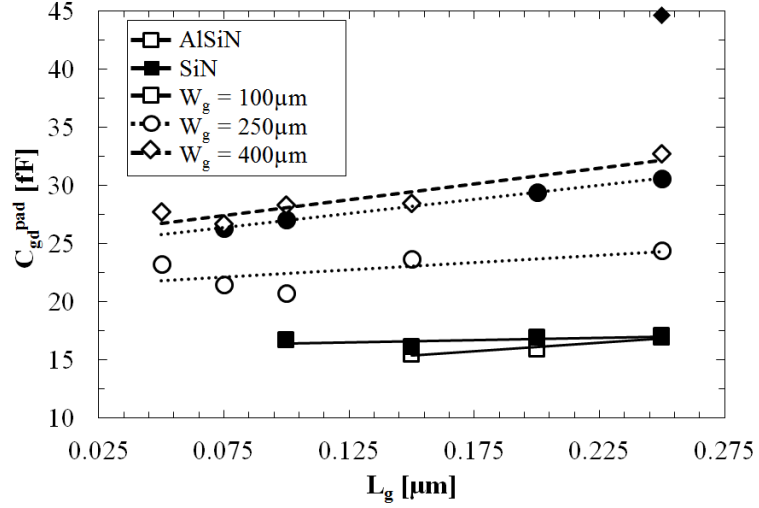


Figure 5.8: Extracted gate-drain pad capacitance plotted against gate length and periphery.

### 5.3.3 Figure of Merit Optimization with Geometry

The maximum value of the extrinsic  $f_T$  recorded was 87 GHz, and the maximum value of the extrinsic  $f_{\max}$  was 150 GHz. The  $f_T$  was optimized at a gate length of 75 nm, and  $f_{\max}$  optimized at a gate length of 200 nm. The AlSiN coated devices consistently had roughly 10 % higher values of these device bandwidth metrics for the same gate dimensions. This is attributed to the reduction of key parasitics. Figures 5.9 and 5.10 show the trends of the extracted intrinsic  $f_T$  and  $f_{\max}$  with gate dimensions for AlSiN-passivated devices. The intrinsic  $f_{\max}$  maximized at the same gate length of 200 nm was 202 GHz for a 100  $\mu\text{m}$  gate periphery. However, intrinsic  $f_T$  maximizes at gate lengths of 100 or 150 nm.

The degradation of both  $f_T$  and  $f_{\max}$  with decreasing gate length is indicative of short-channel effects (SCEs). Short channel effects include a pinch-off voltage shift and increased output conductance. The increase in output conductance leads to degradation of  $f_{\max}$ , while the lateral extension into the drain region of the Schottky depletion region increases the effective length of the gate and causes  $f_T$  to degrade [89]. These effects have been simulated [90,91] and a number of solutions have been suggested. An inverted HEMT structure using N-face GaN [92] is one proposed solution to mitigating drain-induced barrier lowering (DIBL), another scaling effect, though high- $\kappa$  dielectrics would be required to prevent the high gate leakage current caused by the low barrier height between the Schottky gate metal and the GaN. A more commonly proposed solution is to use a “back-barrier”, a thin layer of InGaN or AlGaN, to raise the conduction band level in the buffer [93–95]. The back-barrier helps increase the confinement of the 2DEG in AlGaN/GaN HEMTs and improves the output conductance and pinchoff of short gate length devices. As a result, a 20% higher improvement of  $f_{\max}$  was observed by Palacios et al [93]. This suggests that short-channel effects and DIBL can be mitigated with the use of an appropriate back-barrier.

Furthermore, there is a clear trend of increasing  $f_{\max}$  with decreasing periphery, which can be attributed to decreasing parasitic capacitances, and more notably, the output conductance. The equation for  $f_{\max}$  [73] may be reduced to the simple form,

$$f_{\max} \sim \frac{1}{\sqrt{4G_{ds}R_{in}}}$$

where  $R_{in} = R_s + R_g + R_{gs}$ . From the extracted values of these elements, we observed that  $G_{ds}$  dominates the term because it strongly scales with periphery, dominating  $R_{in}$ , which scales only slightly. For a gate width of  $50 \mu\text{m}$ , we predict an intrinsic  $f_{\max}$  of approximately 260 GHz (Figure 5.11).

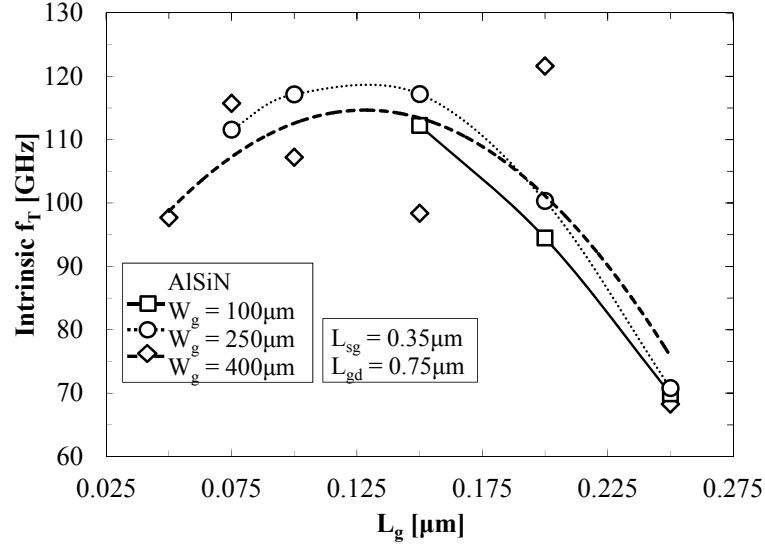


Figure 5.9: Intrinsic  $f_T$  extracted against device gate length. As gate length decreases, the cut-off frequency increases to an optimum at a length of around 100 or 150 nm, beyond which the performance of the device begins to deteriorate.

## 5.4 Large Signal Comparison

Large signal measurements were performed at 10 and 35 GHz on a number of 100  $\mu\text{m}$  and 250  $\mu\text{m}$  gate periphery devices. The input RF signal was swept to the highest power possible before the gate was driven into forward bias. In our measurements, the AlSiN-passivated devices consistently outperformed SiN-passivated devices of identical dimensions. Figure 5.12 shows a typical power sweep for identical devices with different passivations. Not only did the AlSiN devices produce more gain and higher efficiencies, the efficiencies dropped off less sharply with increasing drain bias. This is the principle difference of the performance of devices using the two passivation technologies.

A series of power sweeps were performed with the drain bias increasing in steps of 1 V or 5 V, until the device failed. The results are summarized in

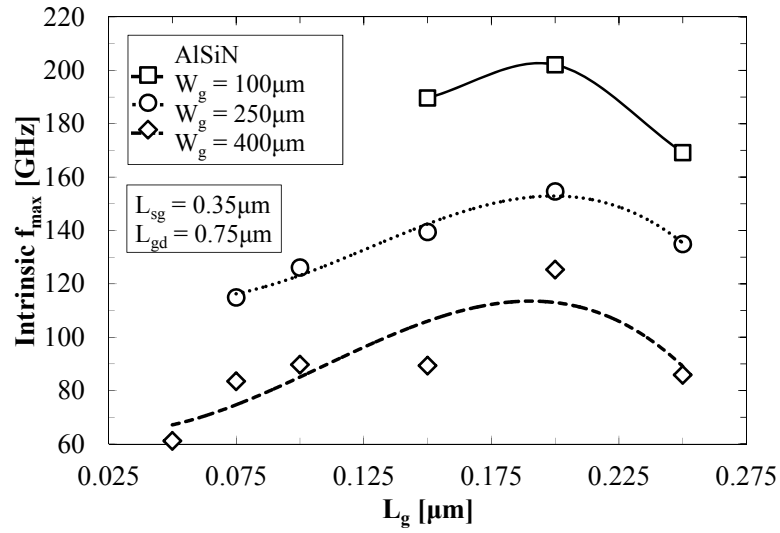


Figure 5.10: Intrinsic  $f_{\max}$  extracted against device gate length. As gate length decreases, the frequency increases to an optimum at a length of 200 nm.

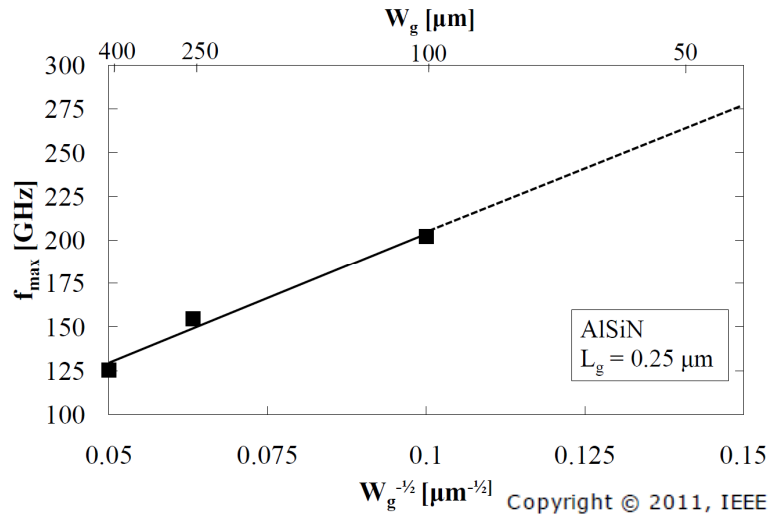


Figure 5.11: Intrinsic  $f_{\max}$  plotted versus inverse gate periphery.

Figures 5.13, 5.14, and 5.15.

The drain bias range reflects the difference between the drain bias tolerance of the two passivations. The AlSiN-passivated devices were consistently able to perform at higher drain biases, as high as 55 V, while the SiN-passivated devices



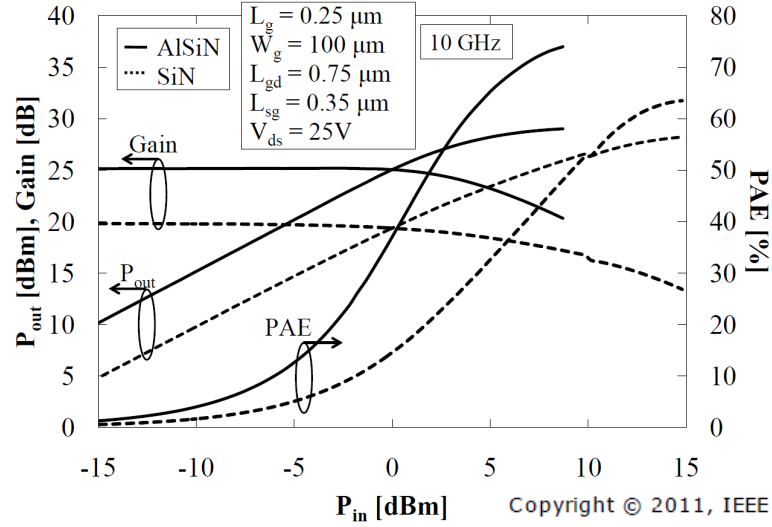


Figure 5.12: Gain, output power, and power-added efficiency as a function of input power for 100  $\mu\text{m}$  gate periphery, 0.25  $\mu\text{m}$  gate length devices of both passivation schemes.

often broke down above 45 V.

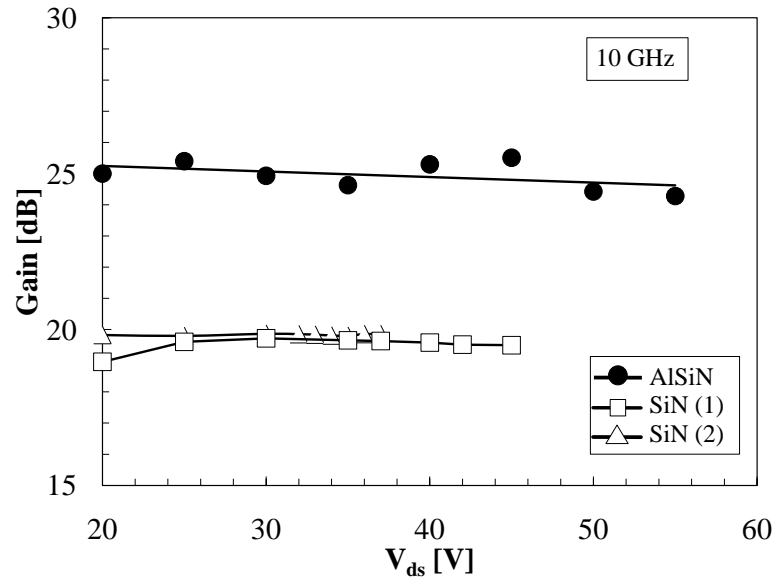


Figure 5.13: Comparison of uncompressed device gain as a function of drain bias for AlSiN- and SiN-passivated devices. SiN(1) refers to an earlier stand-alone sample fabricated by the same process as the SiN(2) and AlSiN samples, which were fabricated side-by-side.

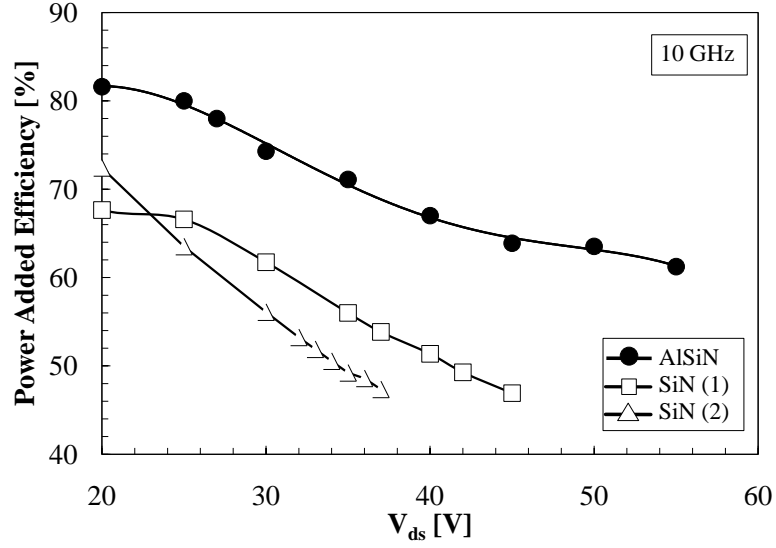


Figure 5.14: Power added efficiency as a function of drain bias for AlSiN- and SiN-passivated devices. SiN(1) refers to an earlier stand-alone sample fabricated by the same process as the SiN(2) and AlSiN samples, which were fabricated side-by-side.

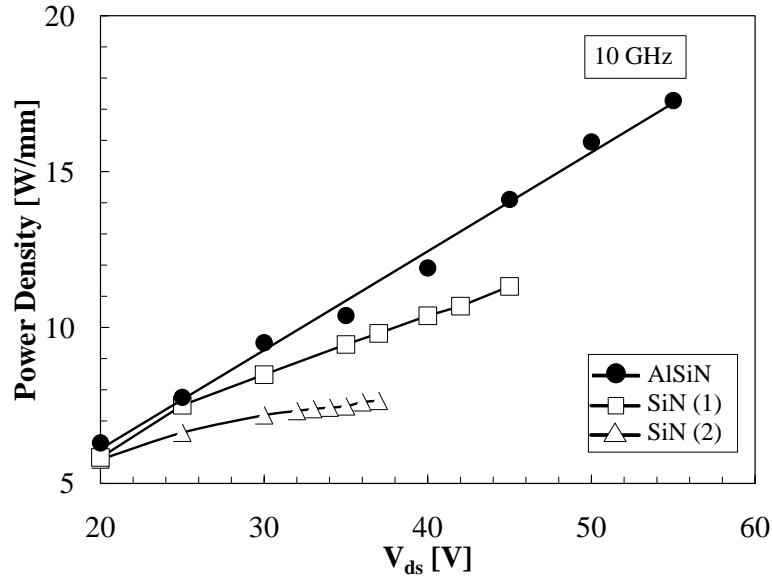


Figure 5.15: Comparison of output power as a function of drain bias for AlSiN- and SiN-passivated devices. SiN(1) refers to an earlier stand-alone sample fabricated by the same process as the SiN(2) and AlSiN samples, which were fabricated side-by-side.

Overall, the AlSiN-passivated devices consistently out-performed the SiN-passivated devices. A maximum PAE of 82% was measured at 15 V on a 100  $\mu\text{m}$  gate periphery, AlSiN-passivated device, with 24 dB of gain. The maximum output power measured was 17.5 W/mm at 55 V on the drain. For the SiN-passivated devices, the maximum PAE was 72.5 % at 15 V, with 20 dB of gain, and the maximum output power was 7.5 W/mm at 37 V on the drain. The decrease in dispersion in the case of the AlSiN passivation is reflected by the significantly higher PAE of those devices at high drain bias. At low bias, the efficiencies of both AlSiN- and SiN-passivated devices are similar, but as drain bias increases, the SiN-passivated devices drop off in efficiency much faster than the AlSiN-passivated devices.

## 5.5 Conclusions

High efficiency HEMTs passivated using AlSiN have been demonstrated. An output power of 17.5 W/mm with a corresponding PAE of 61 % at 10 GHz has been shown at a drain bias of 55 V. These devices also maintained state-of-the-art small signal performance, with close to 90 GHz extrinsic  $f_T$ , and 150 GHz extrinsic  $f_{\text{max}}$ . The AlSiN-passivated devices consistently out-performed their SiN counterparts in both small and large signal measurements.

## CHAPTER 6

### POWER SWITCHING

#### 6.1 Fabrication

The epitaxial structure of the devices consisted of an Al nucleation layer, followed by a 0.5  $\mu\text{m}$  GaN buffer, a 220  $\text{\AA}$  AlGaN barrier with 24.5 % Al fraction, and a 20  $\text{\AA}$  GaN cap grown on semi-insulating SiC. Device fabrication was performed as described in section 2.2. AlSiN was used as the dielectric, with a thickness of 35 nm as determined by ellipsometry. The fabricated devices were dual-gated and had 1.5, 1, or 0.5  $\mu\text{m}$  gate lengths, 400 (2 $\times$ 200)  $\mu\text{m}$  peripheries, and gate-drain spacings of 3 or 5  $\mu\text{m}$ . These features sizes are significant because most high breakdown voltage HEMTs have gate drain spacings in excess of 10  $\mu\text{m}$  [96].

#### 6.2 Device Performance

The methodology and results described in this section have been previously published [58]. DC, small-signal, and large-signal RF measurements were performed. The pinch-off voltage was -5.5 V, and the quiescent point for small and large signal biasing was chosen at the point of maximum transconductance. Figure 6.1 shows the combined DC measurements of the parameter space of a typical device, including the output curves, constant power measurements, and high voltage off-state breakdown measurement. At  $V_{\text{ds}} = 10$  V and  $V_{\text{gs}} = 2$  V, the drain current was approximately 1 A/mm. Constant power measurements (1 W) were taken up to 200 V.

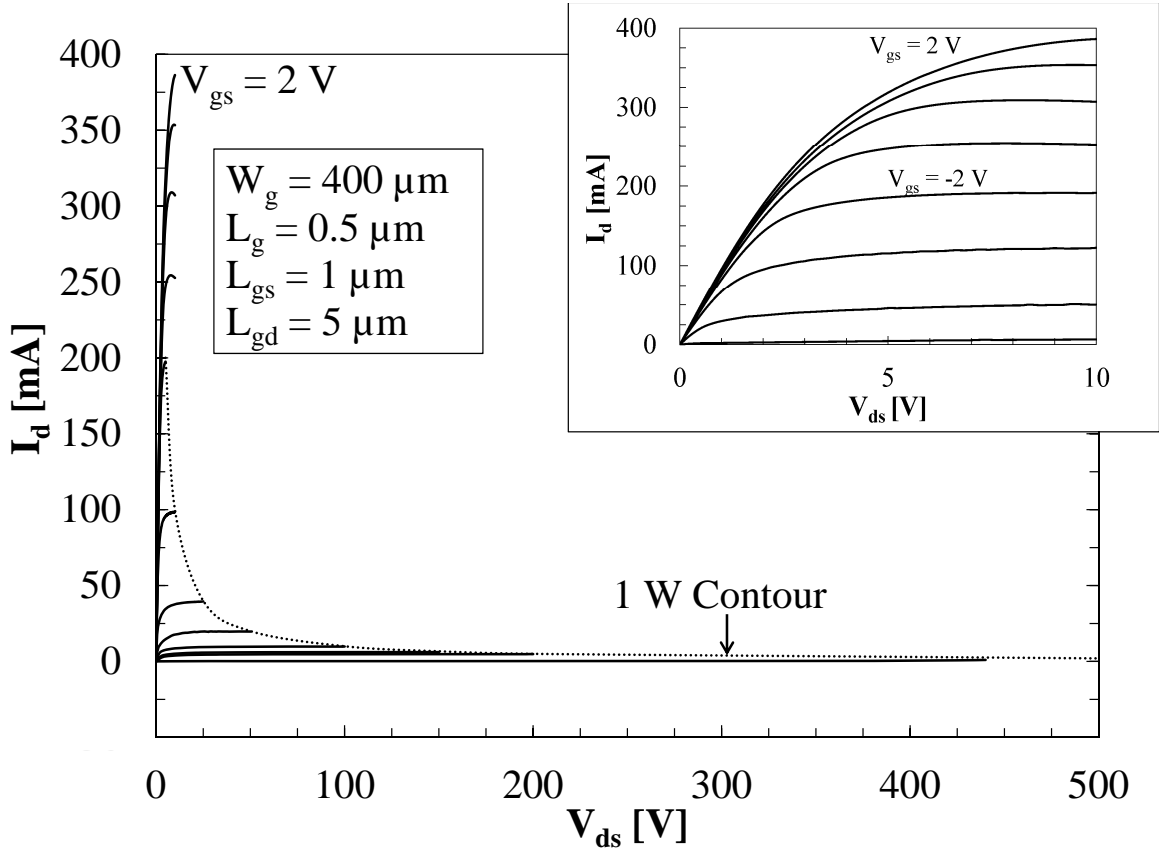


Figure 6.1: Combined DC parameter space measurements. Inset shows the detailed output curves for this device up to 10 V on the drain.

The highest fT of 18 GHz and  $f_{textmax}$  of 40 GHz was obtained on a  $0.5 \mu\text{m}$  gate length device with a  $5 \mu\text{m}$  gate-drain spacing.

Large signal measurements were performed at 10 GHz on a load pull bench. The input was matched for reflection and the output was loaded for maximum efficiency. A typical device power sweep is shown in Figure 6.2, which at  $V_{ds} = 30 \text{ V}$  had 12.2 dB of linear gain, 4.9 W/mm of output power, and 41 % peak power-added efficiency, which is in line with our previous measurements on  $400 \mu\text{m}$  gate width devices of  $0.25 \mu\text{m}$  gate length.

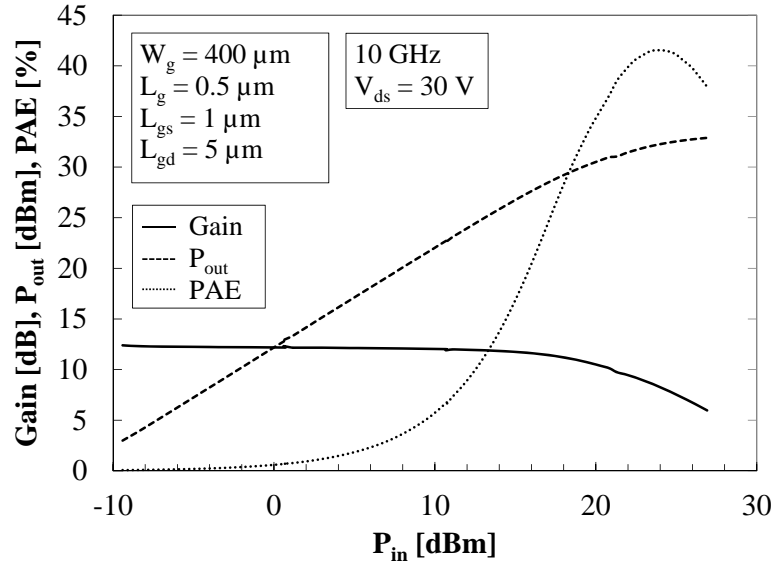


Figure 6.2: Typical 10 GHz load pull power sweep at 30 V of drain bias of a  $0.5 \times 400 \mu\text{m}$  device.

### 6.3 Breakdown Voltage

The off-state breakdown voltage measurement required a number of adjustments. First, because the off-state breakdown measurement is a three-terminal measurement, the standard “U”-device coplanar probe pad layout could not be used as-is. Instead, the sources were connected and the contact pads made larger to facilitate the use of needle probes. Figure 6.3 shows the standard “U” ( 6.3(a)) and modified “O” ( 6.3 (b)) layouts. An HP 4145A Parameter Analyzer was used to supply the gate and source bias, and a Keithley 2410 SMU was used to supply the drain bias and measure the drain current.

For the purposes of the DC high voltage testing, we defined the device off-state breakdown as reaching 1 mA of drain current. The devices were submerged in Diala AX insulating oil to prevent premature air breakdown. With the gate biased at -7 V, breakdown was observed at 440 V for a  $0.5 \mu\text{m}$  gate

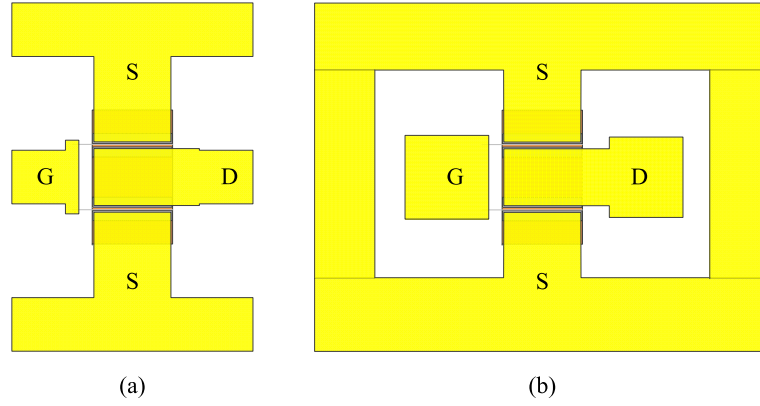


Figure 6.3: Schematic of (a) standard “U” layout for coplanar waveguide probing and (b) modified “O” layout for three terminal off-state breakdown probing.

length device and 470 V for a  $1\ \mu\text{m}$  gate length device, both of which had a source-gate spacing of  $1\ \mu\text{m}$  and a gate-drain spacing of  $5\ \mu\text{m}$  (Figure 6.4). To our knowledge, this is the highest recorded off-state breakdown voltage for an AlGaIn/GaN HEMT device with a relatively small gate-drain spacing and no field plate, exceeding 320 V for a device with similar feature sizes with  $\text{Al}_2\text{O}_3$  passivation [97] and 238 V with SiN passivation [98]. In fact, with our LPCVD SiN passivation, the  $0.5\ \mu\text{m}$  gate length devices typically experience static breakdown at approximately 100 V.

## 6.4 Loadline Analysis

To take the loadline measurements, the loadpull bench was modified to include an HP 71500A microwave transition analyzer (MTA). The diplexer and second harmonic termination branch were removed. The output power meter was replaced by the MTA. On the input side, the narrow-band 40 dB amplifier was replaced by a wider band 20 dB amplifier. Instead of 10 GHz, a 2.5 GHz signal

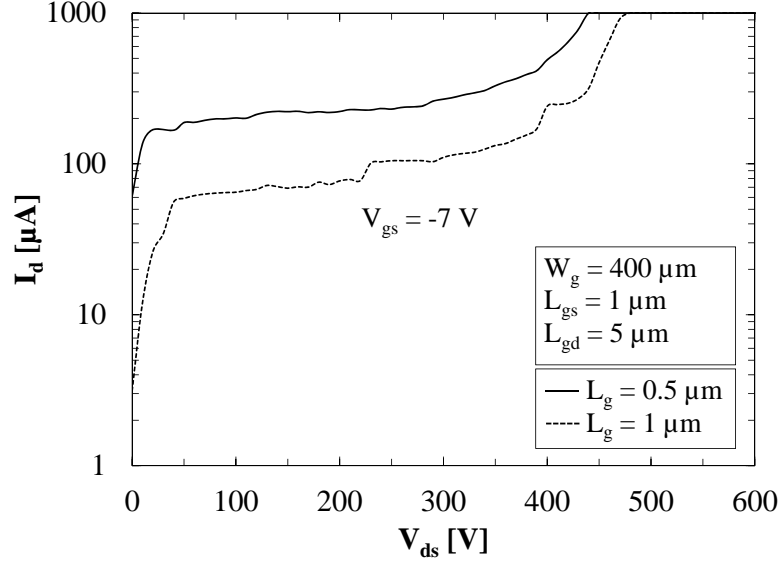


Figure 6.4: Off-state breakdown curve of two  $400 \mu\text{m}$  devices.

was generated so that multiple harmonics could be measured. Figure 6.5 shows the modified bench schematic.

To test switching performance, devices are often measured with the aid of harmonic tuners that change the impedance the device sees on the input and output. The input is usually set to minimize the reflected power to the device, while the output is designed to shape the time domain voltage and current waveforms to get the maximum voltage swing. To observe switching, the device is driven into power saturation, where the drain voltage swings between pinch-off and saturation. When a non-zero reactance is presented to the device output, a delay is induced between the voltage and current waveforms, which results in power dissipation, and “loopiness” in the loadline. These effects increase with increasing reactance. When the reactance is zero, the voltage and current waveforms are exactly out of phase, and the loadline collapses to a straight line.

The goal of these measurements is to observe a loadline on which voltage



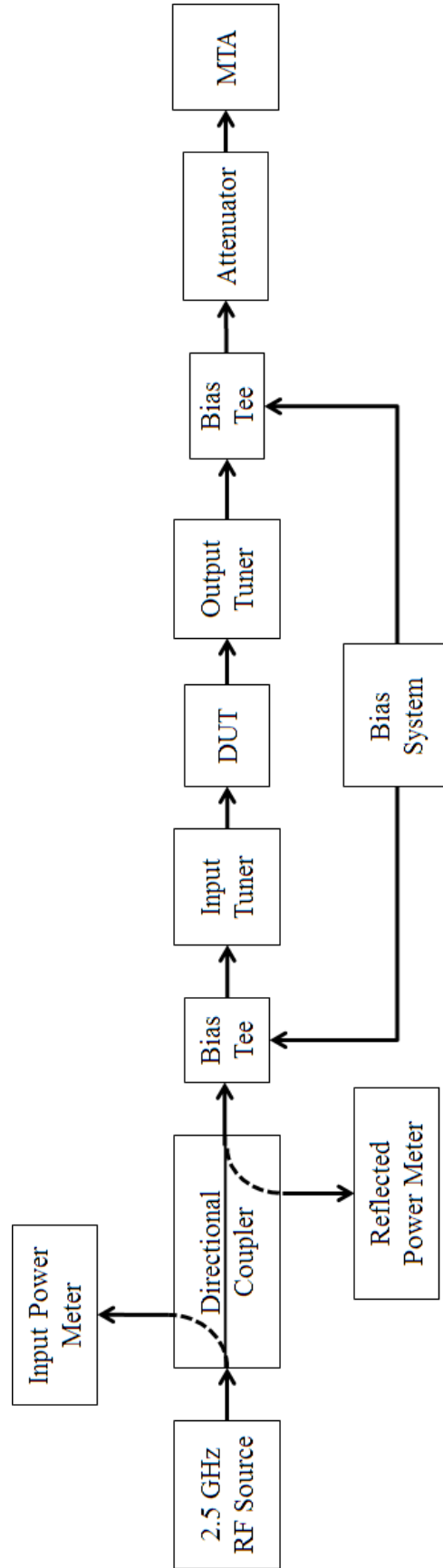


Figure 6.5: Schematic of the modified power bench for loadline measurements at 2.5 GHz. The diplexer and second harmonic branch have been removed, and the output power meters have been replaced by an MTA.

swings between near zero and some large positive value at high drain bias. To test the validity of the time domain transformation to the device plane, a known high efficiency  $0.25 \times 250 \mu\text{m}$  device was tested. The tuner was first set to approximately  $50 \Omega$ . The total load impedance was calculated to be  $58.5 - 12.2i \Omega$ . The gate was biased near pinch-off ( $-10 \text{ V}$ ), and the drain bias was set to  $5 \text{ V}$ . At the maximum power the sweeper and amplifier could deliver, the input power was  $23 \text{ dBm}$ . Figure 6.6 shows the loadline at this setting, with the frequency spectrum of the output signal inset.

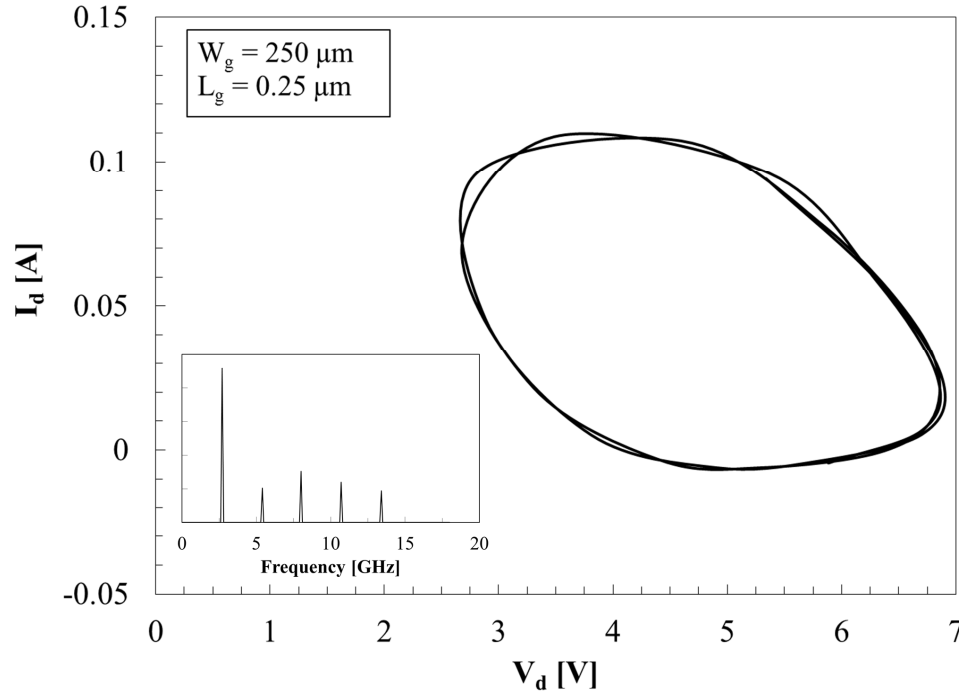


Figure 6.6: Loadline of a  $0.25 \times 250 \mu\text{m}$  device at  $5 \text{ V}$  drain bias and load impedance of  $58.5 - 12.2i \Omega$ , with  $P_{\text{in}} = 23 \text{ dBm}$ .

The tuner was then set to a high impedance value. The load impedance was calculated to be  $90.1 + 117i \Omega$ . Figure 6.7 shows the loadline at the same gate and drain biases and input power as before, with the frequency spectrum of the output signal inset. Note that this signal has a significantly higher second

harmonic component.

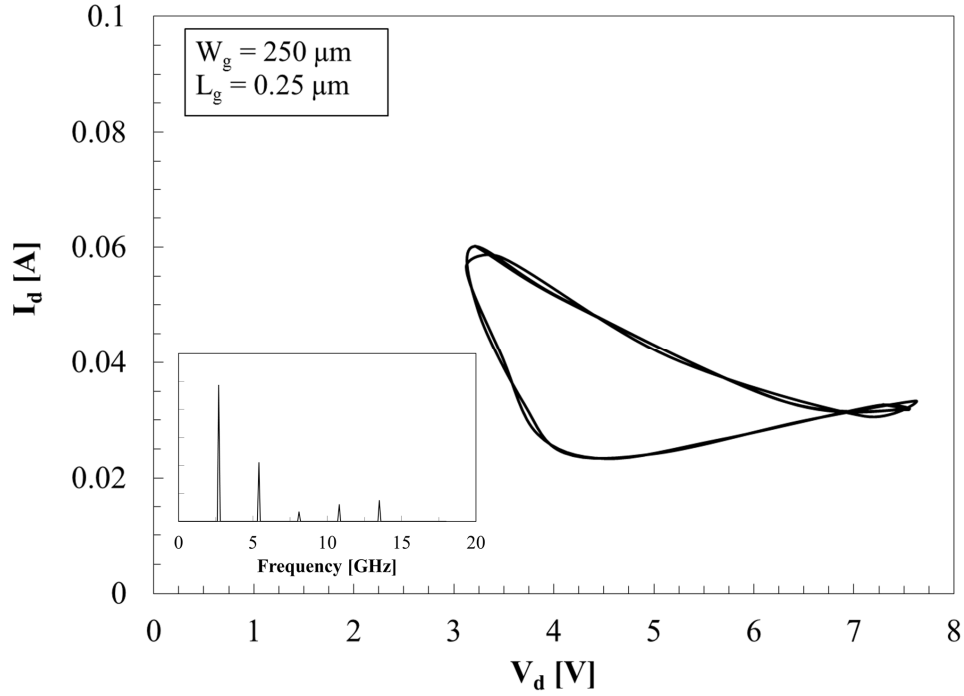


Figure 6.7: Loadline map of a  $0.25 \times 250 \mu\text{m}$  device at 5 V drain bias and a high-impedance tuner setting.

Because the switching behavior was not being observed, it was necessary to determine why. The simplest explanation was simply that there was not enough power being delivered to the device. To confirm this, and that the transformation to the device plane was correct, the above measurements were repeated at 10, 15, and 20 V drain bias. Figure 6.8 shows the results of these sweeps at different drain biases. As we would expect, the loadline ovals simply shift to higher drain biases, and while the swing did increase slightly from approximately 5 to 7 volts, the increase was not significant. This suggests that more power is required to drive the device into pinch-off.

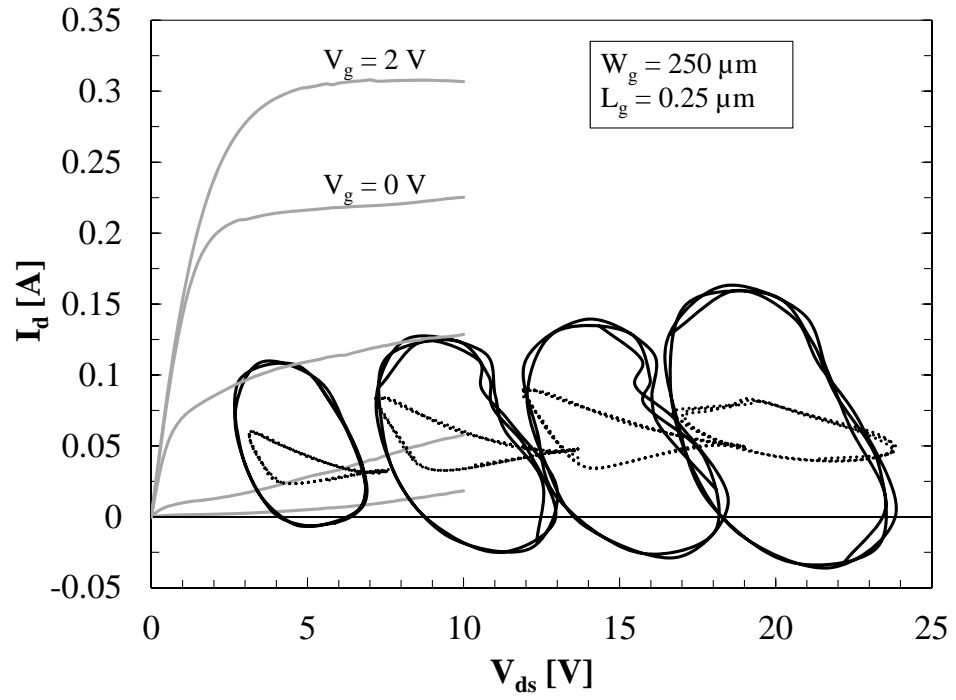


Figure 6.8: Output curves and loadline map of a  $0.25 \times 400 \mu\text{m}$  device at two load impedances and four different drain biases. The drain was biased at 5, 10, 15, and 20 V. The output curves are 2 V steps.

## APPENDIX A

### MATLAB CODE FOR TIME DOMAIN MEASUREMENTS

The following is the code used for the time-domain transformations. Figure A.1 shows the data through the various steps. Section (a) is the data as collected by the MTA, (b) is the frequency spectrum of the MTA data, (c) is the spectrum transformed through the ABCD parameters of the output branch to the DUT plane, (d) is the same spectrum filtered down to the highest peaks, (e) shows the corresponding voltage/current waveforms, and (f) is the loadline.

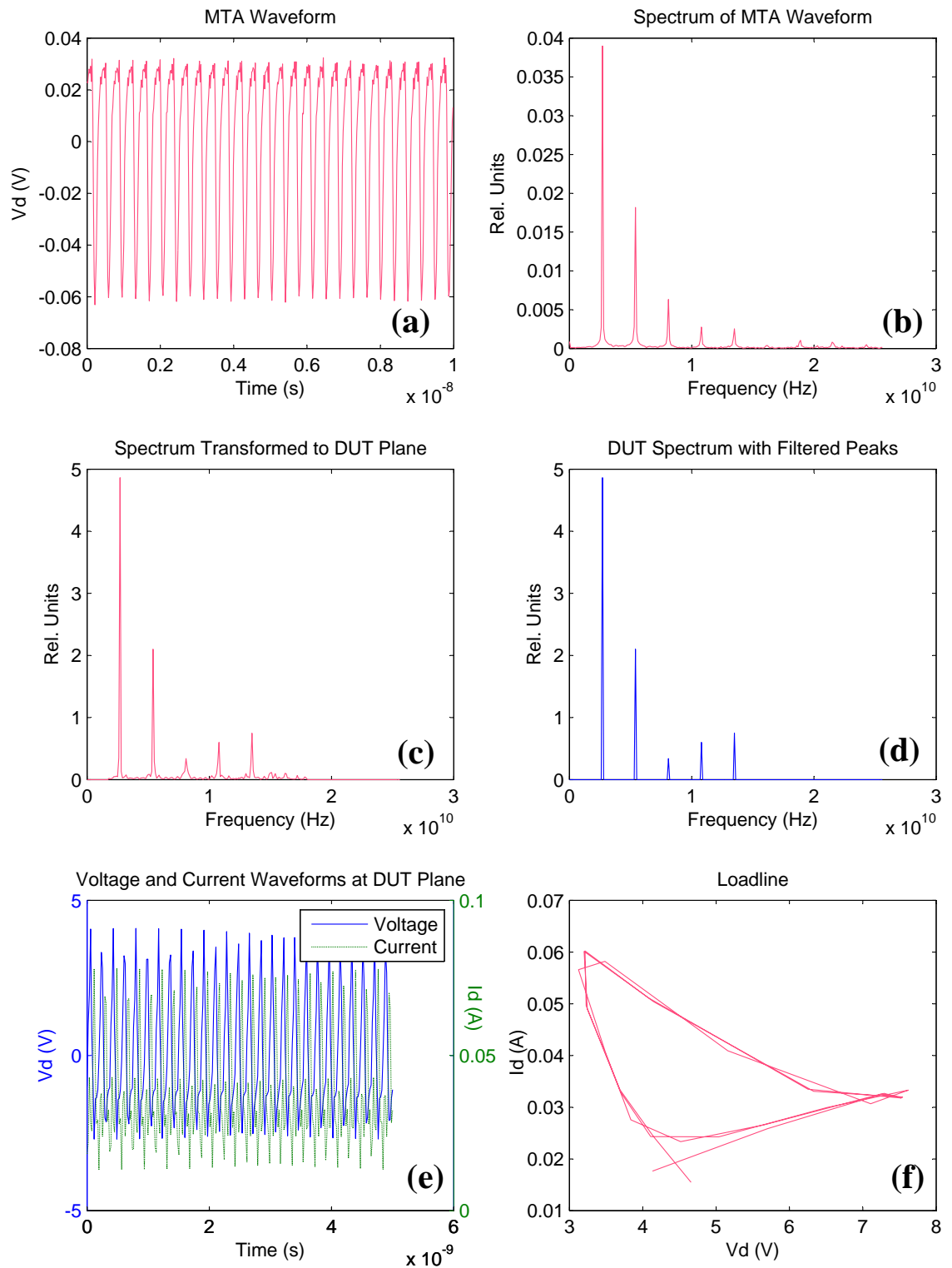


Figure A.1:

```

slide = 2600;      % Enter the slide and probe position of the output tuner
probe = 20;        % These will be used to call the correct files

vg = -10;          % Enter the biasing conditions
vd = 5;            % (also used to call the right file)
power_final = 49;
n=2;

niters = n;                % Used for different color lines for
rvals = linspace(0,1,niters); % each power level
bval = 0.3;
gval = 0.5;

% Build the datafile name from the given info above
vdata = strcat('_',num2str(vg),'V_',num2str(vd),'V_',num2str(power_final),'dB');
dir = '250um/device2/vsweep/'; % Make sure this is the right directory
ifile = '_trange&current';

filev = strcat(dir,'test_',num2str(slide),'_',num2str(probe),vdata,'.txt');
filei = strcat(dir,'test_',num2str(slide),'_',num2str(probe),vdata,ifile,'.txt');
tunerfile = strcat('tuner_data/tuner2_',num2str(slide),'_',num2str(probe),'.s2p');

% Import the tab-delimited data
data = importdata(filev,' ',1);
id = importdata(filei,' ',1);

%Import the calibration data (S-parameters) for the output block
probe = read(rfckt.passive, 'Probe.s2p');
tuner = read(rfckt.passive, tunerfile);

```

```

atten = read(rfckt.passive, 'Atten.s2p');
cable = read(rfckt.passive, 'meas_cable.s2p');

%This is just some stuff Matlab needs to run
freq = [1.8e9:1e8:18e9];
numfreq = numel(freq);           %Different from numf, both used
analyze(probe, freq);
analyze(tuner, freq);
analyze(atten, freq);
analyze(cable, freq);

sparamsprobe = probe.AnalyzedResult.S_Parameters;
sparamstuner = tuner.AnalyzedResult.S_Parameters;
sparamsatten = atten.AnalyzedResult.S_Parameters;
sparamscable = cable.AnalyzedResult.S_Parameters;

%Cascades the S-params
outblock = cascadesparams(sparamsprobe, sparamstuner, sparamsatten, sparamscable);
out1 = cascadesparams(sparamstuner, sparamsatten, sparamscable);

%Convert to ABCD
outABCD = s2abcd(outblock);

for l=2:1:n    % Change if viewing several or one power level

%The sampling time is the time range/number of points, get from data file
%NB, math is easier if the time span gives you a sampling frequency
%that matches your calibration frequency steps

T = 1e-8/512;           %Time range from the data text file
Fs = 1/T;               %Sampling frequency
L = 512;                % Length of signal/number of points
t = (0:L-1)*T;          % Time vector

```



```

vmta_t = data.data(1:512,1);      % the data for a given input power

subplot(3,2,1)
plot(t,vmta_t,'Color', [rvals(1),bval,gval]) % look at it, make sure it's reasonable

xlabel('Time (s)'); y=ylabel('Vd (V)');
title(sprintf('MTA Waveform'));

hold on

NFFT = 2^nextpow2(L);      % Next power of 2 from length, just in case

Vmta_f = fft(vmta_t,NFFT)/L;      % The FFT of the MTA data
Imta_f = Vmta_f/50;      % Corresponding current

numf = NFFT/2+1;      % Only want single sided spectrum
f = Fs/2* linspace(0,1,numf); % The frequency range

subplot(3,2,2)      % Frequency spectrum of the MTA data
plot(f,2*abs(Vmta_f(1:numf)),'Color', [rvals(1),bval,gval]);
xlabel('Frequency (Hz)'); y=ylabel('Rel. Units');
title(sprintf('Spectrum of MTA Waveform'));

hold on      % Should show the harmonic peaks

%Start with the DUT data as just all the mta data
Vdut_f = Vmta_f;
Idut_f = Imta_f;

count = 1;

```

```

%Transform only those frequencies that are calibrated for

for i=1:numf

    if freq(1)<=f(i)&&f(i)<=freq(numfreq) % In cal range?

        %NB this gets messy if the sampling freq step != cal freq step

        Vdut_f(i) = outABCD(1,1,count)*Vmta_f(i)+outABCD(1,2,count)*Imta_f(i);

        Idut_f(i) = outABCD(2,1,count)*Vmta_f(i)+outABCD(2,2,count)*Imta_f(i);

        count = count + 1;

    else %If not in range, it's 0

        Vdut_f(i) = 0;

        Idut_f(i) = 0;

    end

end

%The transformed spectrum

subplot(3,2,3)

plot(f,2*abs(Vdut_f(1:numf)),'Color', [rvals(1),bval,gval]);

xlabel('Frequency (Hz)'); ylabel('Rel. Units');

title(sprintf('Spectrum Transformed to DUT Plane'));

hold on

%Filter the harmonic peaks

%MINPEAKDISTANCE forces it to ignore little peaks around the big peaks

spectrum = 2*(abs(Vdut_f(1:numf)));

[pks,locs] = findpeaks(spectrum,'MINPEAKDISTANCE',10,'npeaks',5);

%Make an array of zeroes, will fill in with filtered spectrum

Vdut_ff = zeros(1,numf); % The extra f is for filtered : Idut_ff = zeros(1,numf);

```

```

count = 1;

for i=1:NFFT

    if count <= numel(locs) && i==locs(count) %if this is an index of a peak

        Vdut_ff(i) = Vdut_f(i);           %assign the value of the spectrum

        Idut_ff(i) = Idut_f(i);

        %Calculate the impedance looking into the output block at each peak

        ZIN(count) = -50*(outblock(1,1,i)+1)/(outblock(1,1,i)-1);

        count = count + 1;

    end

end

specff = 2*abs(Vdut_ff(1:numf)); % The filtered spectrum

subplot(3,2,4)

plot(f,specff);

xlabel('Frequency (Hz)'); ylabel('Rel. Units');

title(sprintf('DUT Spectrum with Filtered Peaks'));

% BY THE POWER OF GREYSKULL

vdut_t = ifft(Vdut_ff,numf)*L/2;           % Back to time domain!

idut_t = ifft(Idut_ff,numf)*L/2;

subplot(3,2,5)

% Adjust for the DC levels

[AX,H1,H2] = plotyy(t(1:numf),vdut_t, t(1:numf),(id.data(1)-idut_t),'plot');

set(get(AX(1),'Ylabel'),'String','Vd (V)')

set(get(AX(2),'Ylabel'),'String','Id (A)')

```

```

set(H2, 'LineStyle',':');
legend('Voltage', 'Current');
xlabel('Time (s)');
title(sprintf('Voltage and Current Waveforms at DUT Plane'));

hold on

% Smooth the data out a bit, only take the first 3 or so periods

x = smooth(abs(vdut_t(1:30)).*cos(-angle(vdut_t(1:30)))+vd,'lowess');
y = smooth(-abs(idut_t(1:30)).*cos(-angle(idut_t(1:30)))+id.data(1),'lowess');

subplot(3,2,6)
% This better look not stupid!
plot(x, y,'Color', [rvals(1),bval,gval]);
xlabel('Vd (V)'); ylabel('Id (A)');
title(sprintf('Loadline'));

hold on

end

```

## APPENDIX B

### LOAD-PULL BENCH USER'S MANUAL

#### **B.1 Introduction**

##### **B.1.1 Purpose**

The purpose of this manual is to describe the setup and operation of the Shealy lab RF load-pull large signal measurement system. This manual will go through the individual components of the power bench, its calibration, and operation via IC-CAP. General day-to-day use is covered; for advanced troubleshooting or upgrades, please refer to the user's manual of the component which needs to be serviced.

##### **B.1.2 Description**

In broad terms, the load-pull power measurement system consists of two sources—DC and RF—which provide the drive to the device, tuners on the input and output which adjust the impedance of the source and load, and power sensors that measure the power at various sections of the system. Figure B.1 shows the physical layout of the power bench in the lab, while Figure B.2 shows a block schematic of the components.

The RF signal is generated by the HP8350B Sweep Oscillator and goes through the 40dB solid state amplifier. The signal level is then controlled by the HP 11713A stepped attenuator, which provides up to 80dB of attenuation.

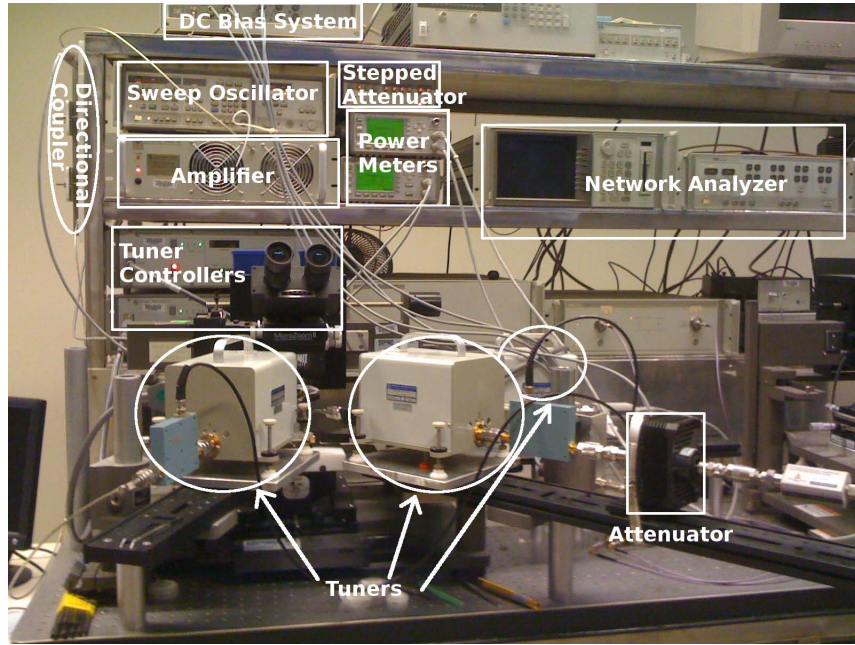


Figure B.1: The power bench and its components.

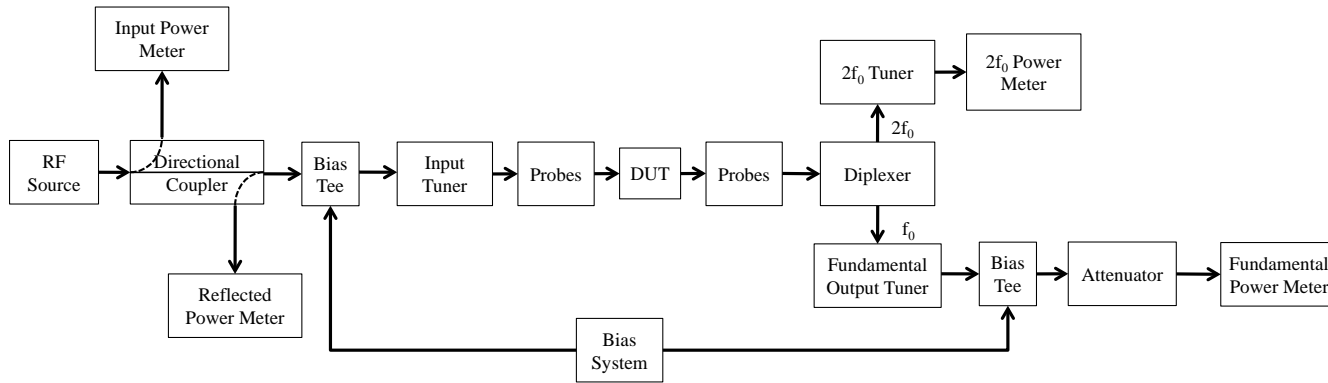


Figure B.2: Block Schematic of Load-Pull Bench

The oscillator has a 10dB swing, so the range of the RF signal typically used is -40dBm to 30dBm. The signal is fed into the “input” port of the directional coupler, which provides two outputs for the incoming signal—the “test” port and “incident” port. The “incident” port is connected to the “A” port of the bottom

Component	Manufacturer	Model Number
DC Bias	Agilent	4142B
Bias Tee (input)	Teleplex Inc.	9460-9-5757
Bias Tee (output)	Maury	9690A
RF Sweeper Oscillator	Hewlett-Packard	8350B
Stepped Attenuator	Hewlett-Packard	11713A
Amplifier	Microwave Power	C1010-40-R155
Directional Coupler	Hewlett-Packard	11692D
Fundamental Tuner	Maury	MT982A
Second Harmonic Tuner	Maury	MT983A
Tuner Controller	Maury	MT986B
30dB Attenuator	Agilent	8498A
Power Meter	Agilent	E4419 B
Coplanar Waveguide Probes	Cascade Microtech	FPC-GSG-250

power meter for determining the input power. The “test” port output continues to the bias tee and tuner via a cable. The power reflected from the device travels back through the same cable and is measured through the “reflected” port, which goes to the “B” port of the bottom power meter. See Figure B.3 for directional coupler port layout.

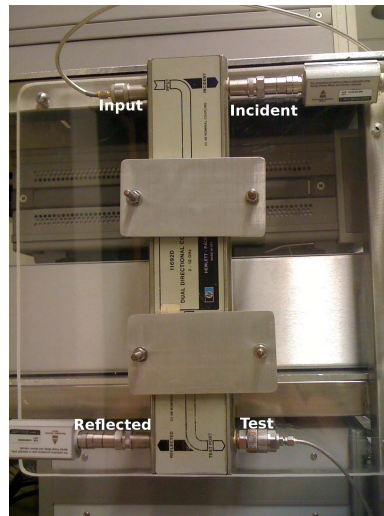


Figure B.3: The directional coupler ports.

In order to operate the power bench, the S parameters of all components

must be determined in the frequency range to be used. This is done by direct measurements of small-signal S parameters using the Network Analyzer (NWA).

## B.2 Small Signal Calibration/Measurements

### B.2.1 The HP8510C Network Analyzer

Before calibrating the network analyzer (NWA), familiarize yourself with the front panel, especially the keys highlighted in Figure B.4.

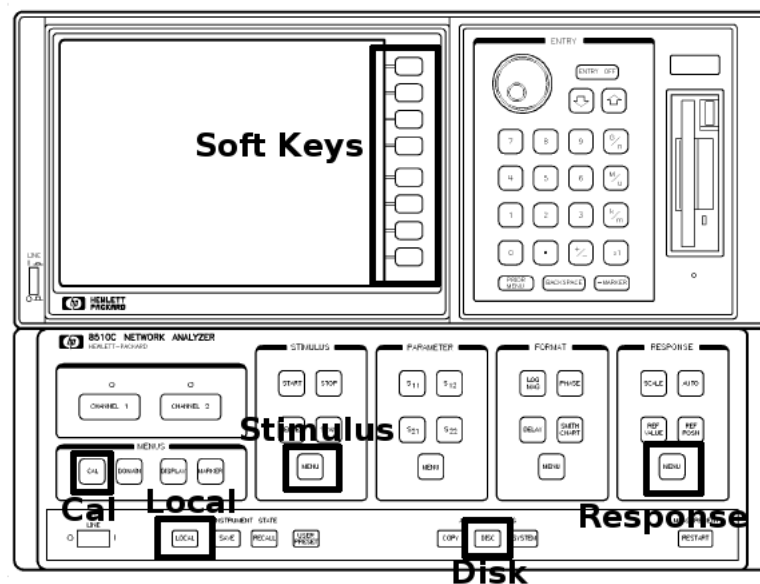


Figure B.4: Schematic of the HP8510C NWA front panel.

The calibration kit used will depend on the type of connector. The components on the input side of the device and the fundamental output branch use 7mm hermaphroditic connectors, while the second harmonic output branch



uses 3.5mm connectors. However, the calibration procedure is essentially the same for either connector size.

## **B.2.2 NWA Setup**

Before you can begin calibrating the NWA, you must first set the hardware options to the correct calibration kit (3.5 mm or 7 mm), and configure the NWA for your chosen frequency range.

### **Choose your kit**

1. Check that the Cal Kit Data disk is in the drive.
2. Press the `LOCAL` key.
3. Press `DISK`.
4. Select `LOAD` (Softkey 3).
5. Select `CAL KIT 1-2` (SK7).
6. Select which cal kit position you want to overwrite with the cal kit you're about to select. For simplicity, choose `CAL KIT 2` (SK2), and always keep the on-wafer kit as cal kit 1.
7. Use the arrow in the `ENTRY` block to select `CK_3_5_MM` or `CK_7_MM`.
8. Select `LOAD FILE` (SK8).

## Set the Frequency and Power

The frequency and power settings can be set either directly on the NWA, or more simply in IC-CAP. To use IC-CAP, first open any CAL model.

1. In the Select DUT/Setup pane, select the first DUT, seven\_mm\_Cal.
2. In the Measure/Simulate tab, select the frequency input block.
3. Set the start and stop frequency you want. See Figure B.5.

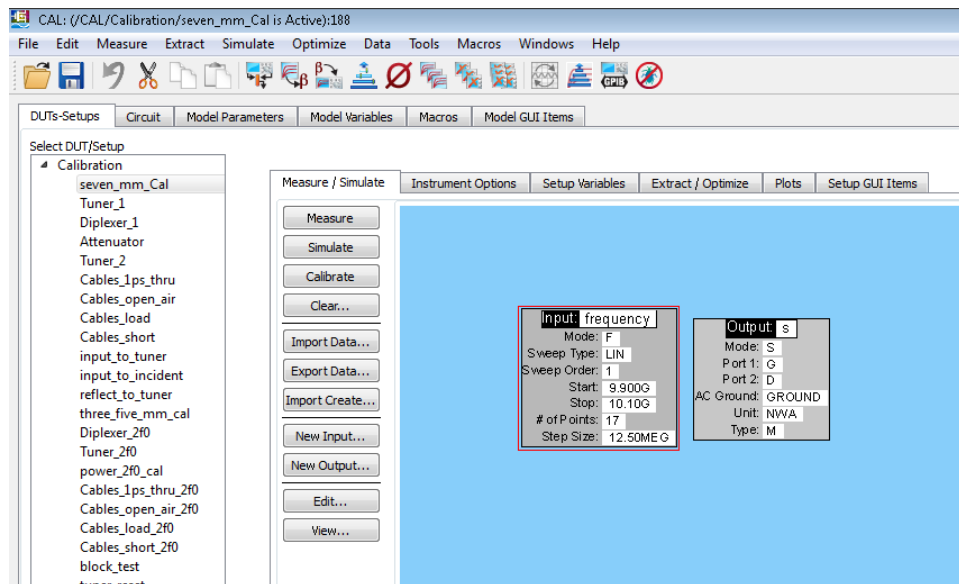


Figure B.5: Setting the sweep frequency in the frequency block.

4. In the Instrument Options tab, set your desired power settings. The default settings are shown in Figure B.6. Note that the Cal Set number is 1, which is where the setup will be downloaded to.
5. Make sure that the Cal Type is set to H, for Hardware calibration.

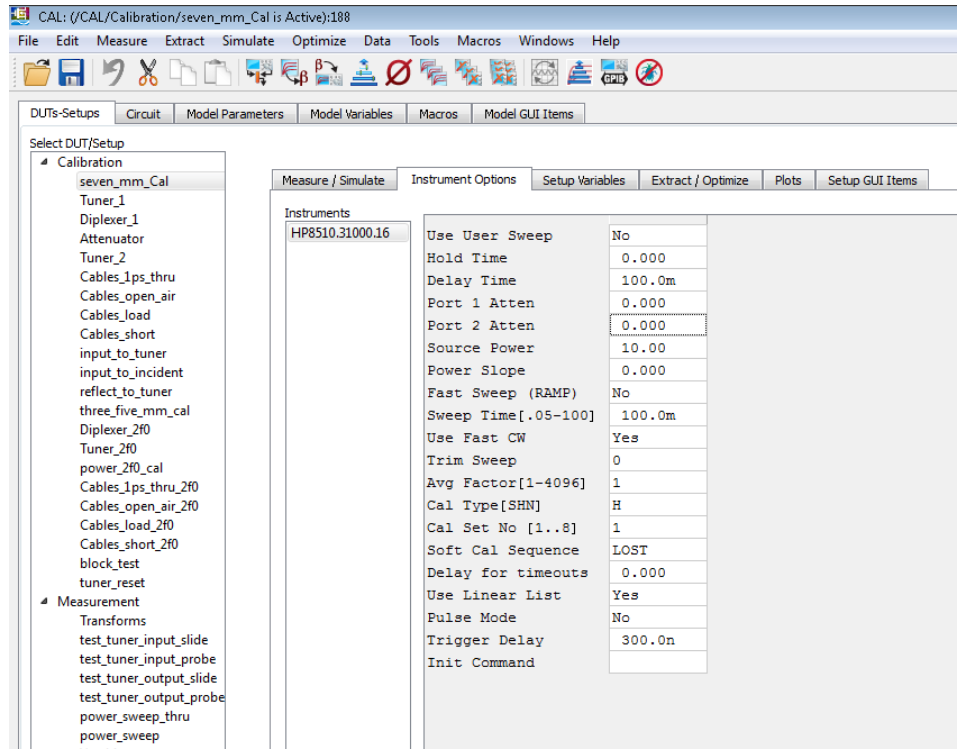


Figure B.6: Power Menu.

6. Back in the Measure/Simulate tab, hit the Calibrate button. You will get a message stating that you are about to download the frequency setup into the NWA (Figure B.7).
7. Hit Ok.
8. You will get a message telling you to calibrate the NWA and then hit ok.
9. You should now perform the hardware calibration of the NWA.

### B.2.3 Calibration

The following procedure describes how to calibrate the HP8510C Network Analyzer using either the 3.5 or 7 mm calibration kit.

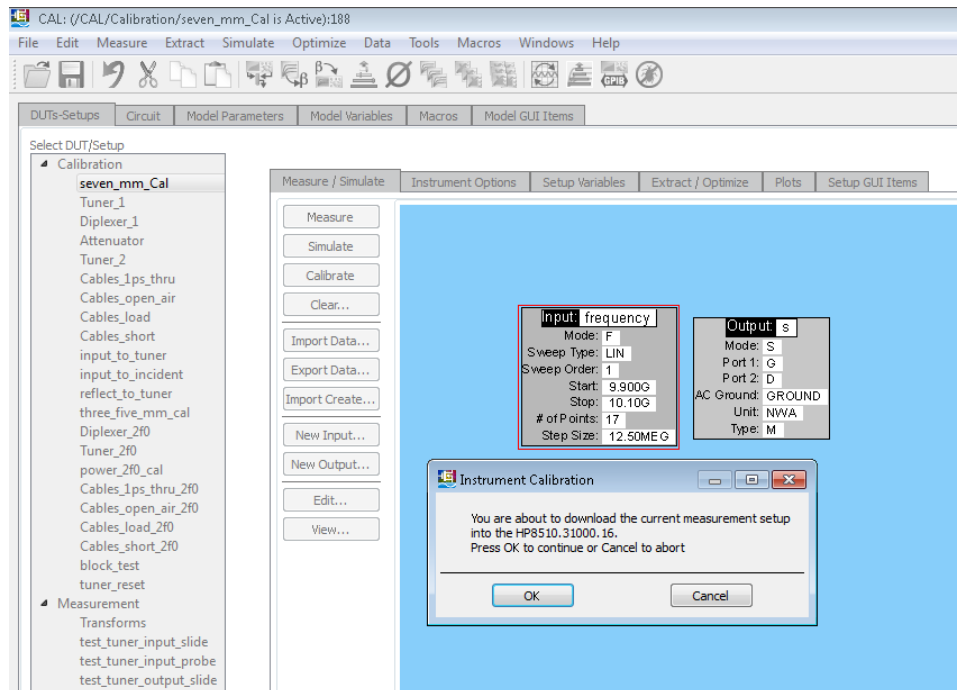


Figure B.7: Downloading the Calibration setup.

In general, when a measurement is completed, the corresponding soft key will be underlined. The exception is the sliding load which is measured repeatedly for several positions of the slider. When using the sliding load, make sure one measurement is completed before commencing the next one.

The sliding load is used to separate the load's reflection from other reflections in the system, improving the corrected system's directivity. The magnitude of the load reflection is constant, but the phase changes as the slide is moved. It is therefore important to not use equidistant slide positions during calibration. To make sure this is avoided, there are marks along the length of the sliding load that should be used for positioning. These marks can be felt when the slide is moved over them and sets into place. If it is hard to feel this, the slide should be positioned with the marks aligned with its lower edge to

maintain non-equidistant positions.

When calibrating using the sliding load, the slide should initially be positioned at the mark closest to the middle. A measurement is made by selecting `SLIDE IS SET` (SK1) on the NWA. Once a measurement is taken, the slide is moved to the next mark, and the next measurement is taken. The slide should only be moved in one direction during the calibration to ensure repeatability.

#### 1. Initialize the calibration

- (a) Press `LOCAL`, followed by `CAL`.
- (b) Select `OFF` (SK2) to disable the previous correction.
- (c) Select `CAL 1/2 3.5mm` or `CAL 1/2 7mm` (SK5/6) depending on the kit you are using and which position it is in.
- (d) Select `FULL 2-PORT` (SK7).

#### 2. Reflection

- (a) Select `REFLECTION` (SK1)
- (b) Connect the Open standard to Port 1 and select `(S11) OPEN` (SK1).
- (c) Connect the Short standard to Port 1 and select `(S11) SHORT` (SK2).
- (d) Connect the Open standard to Port 2 and select `(S22) OPEN` (SK4).
- (e) Connect the Open standard to Port 1 and select `(S22) SHORT` (SK5).
- (f) Connect the Sliding Load to Port 1 and select `(S11) LOADS` (SK3).
- (g) Set the slide to the marker closest to the middle and select `SLIDE IS SET` (SK1).
- (h) Repeat for the remaining markers on the Sliding Load.

- (i) When finished, hit `SLIDING LOADS DONE` (SK8).
- (j) Select `DONE LOADS` (SK8).
- (k) Repeat the Sliding Load calibration for Port 2.
- (l) Select `REFLECTION DONE` (SK8).

### 3. Isolation

- (a) Select `ISOLATION` (SK3).
- (b) Connect the precision  $50\Omega$  standards to Ports 1 and 2.
- (c) Select `FORWARD ISOLATION` (SK5), and then `REVERSE ISOLATION` (SK6).
- (d) Select `ISOLATION DONE` (SK8).

### 4. Transmission

- (a) Select `TRANSMISSION` (SK2).
- (b) Connect Ports 1 and 2 together to form a zero-length thru.
- (c) Select each of the options: `FWD. TRANS. THRU` (SK2), `FWD. TRANS. THRU` (SK3), `FWD. TRANS. THRU` (SK4), `FWD. TRANS. THRU` (SK5).
- (d) Select `TRANS. DONE` (SK8).

### 5. Verification

- (a) In IC-CAP, select `seven_mm_cal` or `three_five_mm_cal` under the Calibration DUT in the DUT/Setup pane.
- (b) Ensure that the frequency and power settings match what you downloaded into the NWA originally, then hit `Measure`.

- (c) In the `Plots` tab, examine the s-parameter plots by double clicking on each.
- (d) Figure B.8 has examples of good calibration plots. The magnitudes of both  $S_{11}$  and  $S_{22}$  should be large and negative ( $< -50$  dB), while the magnitudes of  $S_{12}$  and  $S_{21}$  should be small ( $< 0.1$  dB).

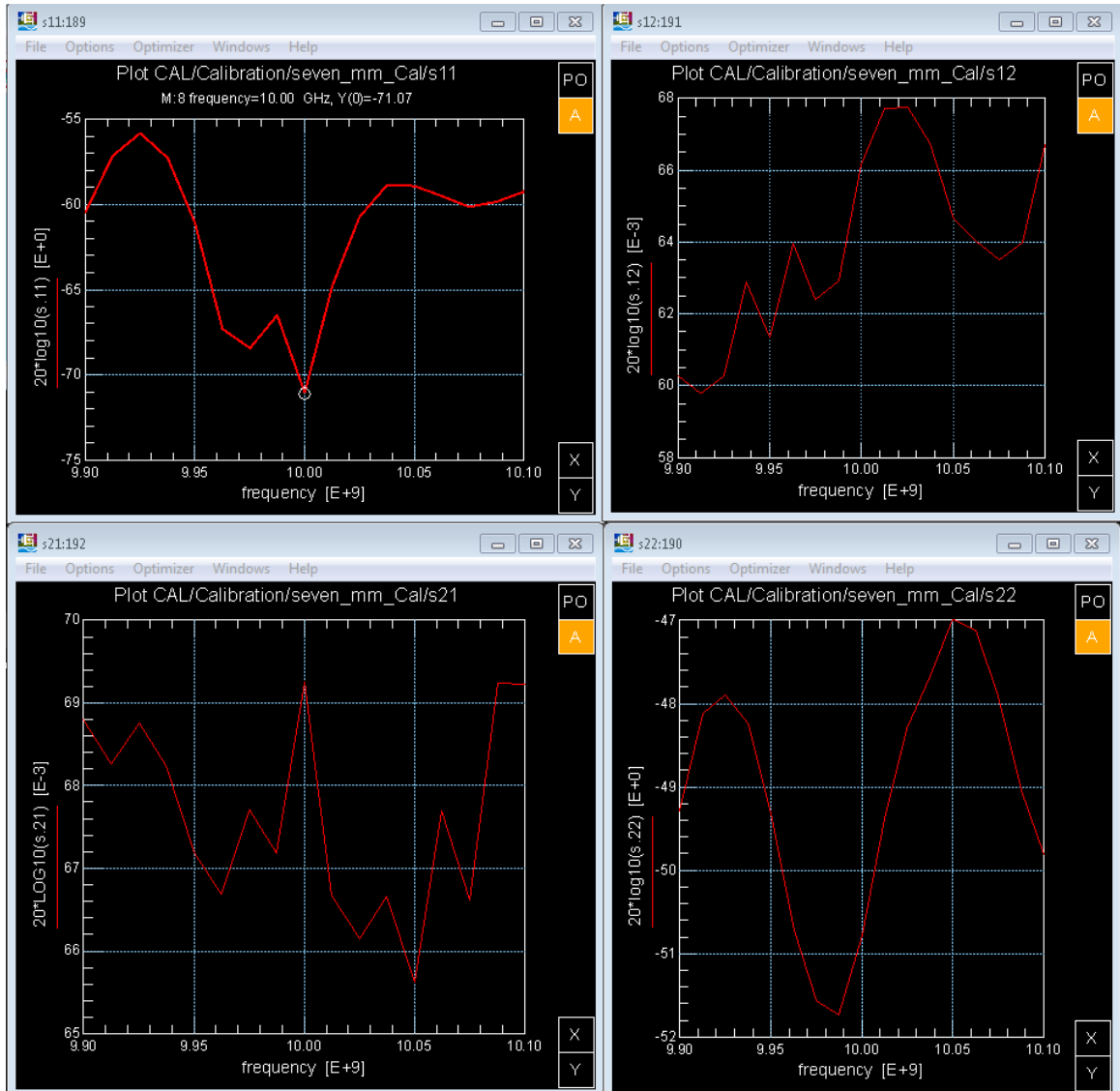


Figure B.8: Calibration verification plots.



## B.2.4 Calibrating the Bench

### Taking it Apart

It's easiest to first calibrate everything that isn't a tuner, starting at the farthest piece (directional coupler) and following the signal flow to the attenuator.

### Directional Coupler

You will probably need to remove the directional coupler from its rack, and this is easiest with two people. You can avoid doing this by calibrating really long cables to reach all the ports if you want. First, disconnect the power meters and RF source line from the coupler, but keep the cable that goes to the tuner on the "Test" port. While one person holds on to the coupler, loosen the screws that hold the coupler's rack. You only need to completely undo the screws on one side.

1. Find 7 mm to N-type adapters for both ports. Yes, this will ever-so-slightly affect the measurement. No, it shouldn't be a big enough difference to be important.
2. Connect Port 1 to the "Input" port on the coupler. Connect Port 2 to the "Incident" port on the coupler. For all coupler measurements, the first port listed in the Setup pane (Figure B.9) is Port 1, and the second is Port 2. In the figure, you can see this measurement is called `input_to_incident`.
3. Again, make sure the frequency block is set to the correct range and that the power settings in the instrument options tab are the same as what you used to calibrate the NWA.

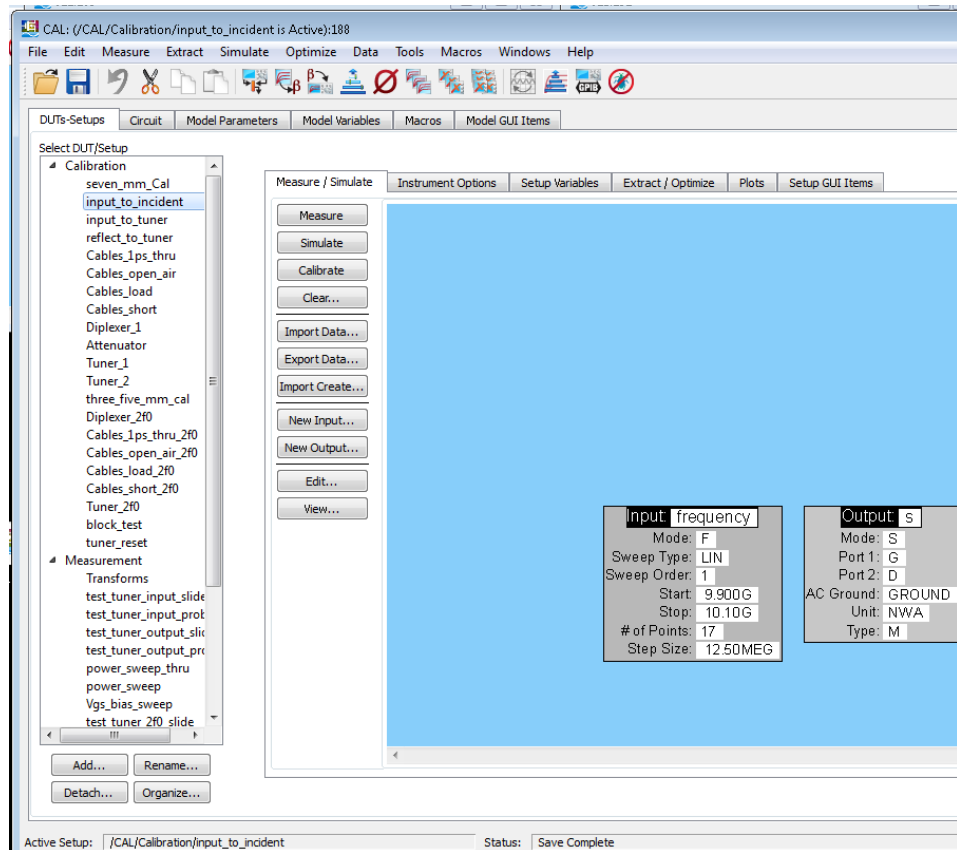


Figure B.9: Setup pane, with suggested order of measurements.

4. Select Measure.
5. Inspect the plots, keeping in mind that there should be about 22 dB of coupling between the input and incident ports.
6. Repeat for the `input_to_test` setup. You'll have to remove the adapter from Port 2 to attach it to the end of the cable on the "Test" port.
7. Repeat for the `reflect_to_tuner`. Port 1 is on "Reflect," Port 2 is still on the "Test" cable.
8. Re-mount the coupler when you're done, and re-attach the power meter and RF source lines.

## Cables and Probes

1. First, you'll need to disconnect the cables from the input tuner and diplexer. Make sure that the probes are UP (not contacted to anything) and AWAY from each other. While you're doing this, it's a good idea to disconnect the diplexer from both output tuners. See Figure ?? for connections.

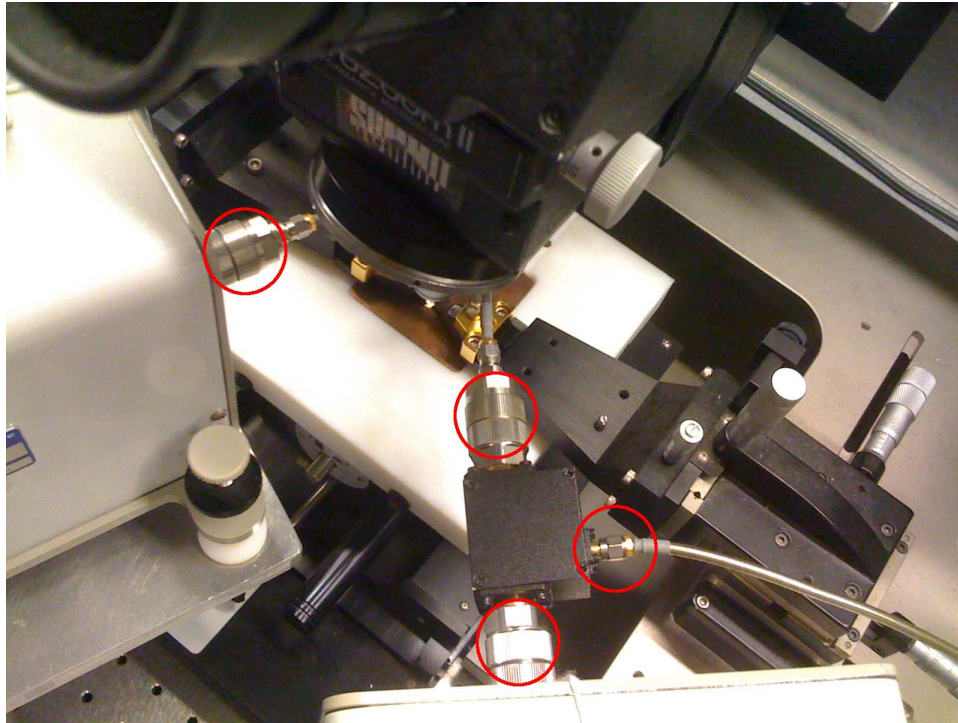


Figure B.10: Stage connection points.

2. Connect Port 1 to the left set of probes, next to the input tuner, and Port 2 to the right set of probes, next to the diplexer and output tuners.
3. You will need to take 4 sets of measurements using the calibration standard which should be on the stage.
4. Probe a 1 ps thru-line, make sure the frequency and power settings are

correct, and hit Measure.

5. Lift the probes completely to do the `open_air` measurement.
6. Probe and measure a short standard.
7. Probe and measure a  $50\ \Omega$  standard.
8. For each of these measurements, go into `Extract/Optimize` tab and execute all the transforms by double clicking.
9. Back in the `Cables_1ps_thru` Setup, you'll be able to see the measured and modeled values of the S-parameters (Figure B.11. Inspect the plots to make sure they're reasonable.

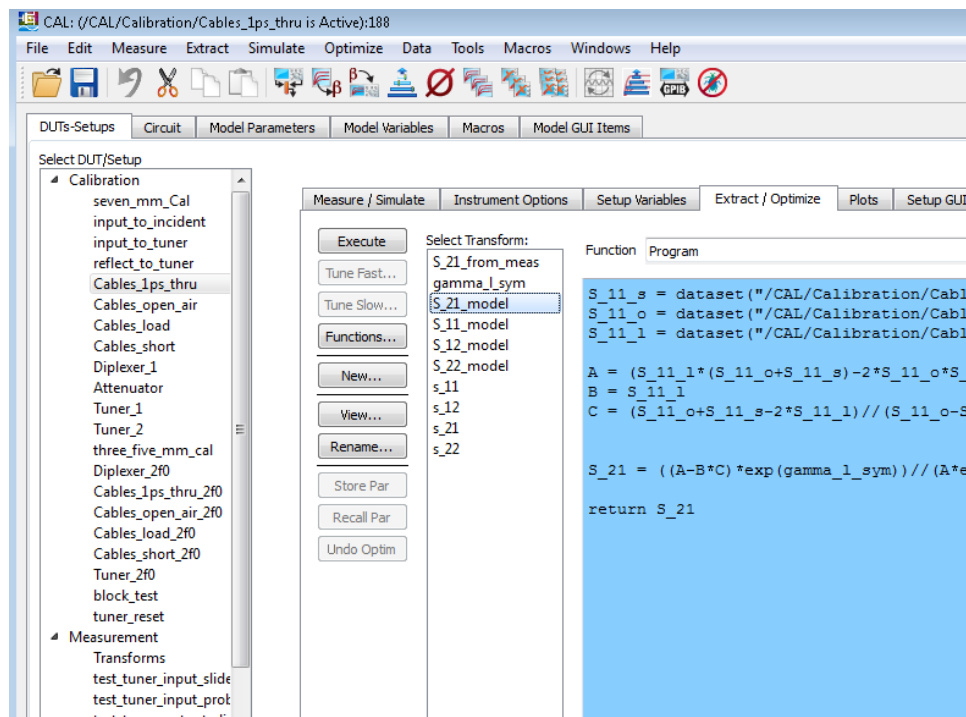


Figure B.11: Cable model transforms.

## Diplexer and Attenuator

These are pretty simple, just make sure you follow the signal flow. The input side of the Diplexer (for Port 1) is marked as `COMMON` and the fundamental output (Port 2) side is marked as `F0`.

1. Connect Ports 1 and 2 to the input and output of the Diplexer.
2. Check the frequency/power settings and `Measure`.
3. Connect the ports to the attenuator, check power settings, and `Measure`.
4. Check the plots for each.

## Tuners

Here the procedure changes slightly.

1. Select the `Setup` of the tuner you are calibrating, and select the `Measure/Simulate` tab.
2. In the `frequency` input block, set a constant frequency at which you will be calibrating. In Figure B.12, for example, this frequency is 10 GHz.
3. In the `Slide` input block, set the tuner slide start, end, and step. The values in Figure B.12 will give a good mesh. Your goal is to cover as much of the Smith Chart as possible.
4. Do the same for the `Probe` values.
5. Once you're all set, check the power settings.
6. You can now `Measure`.

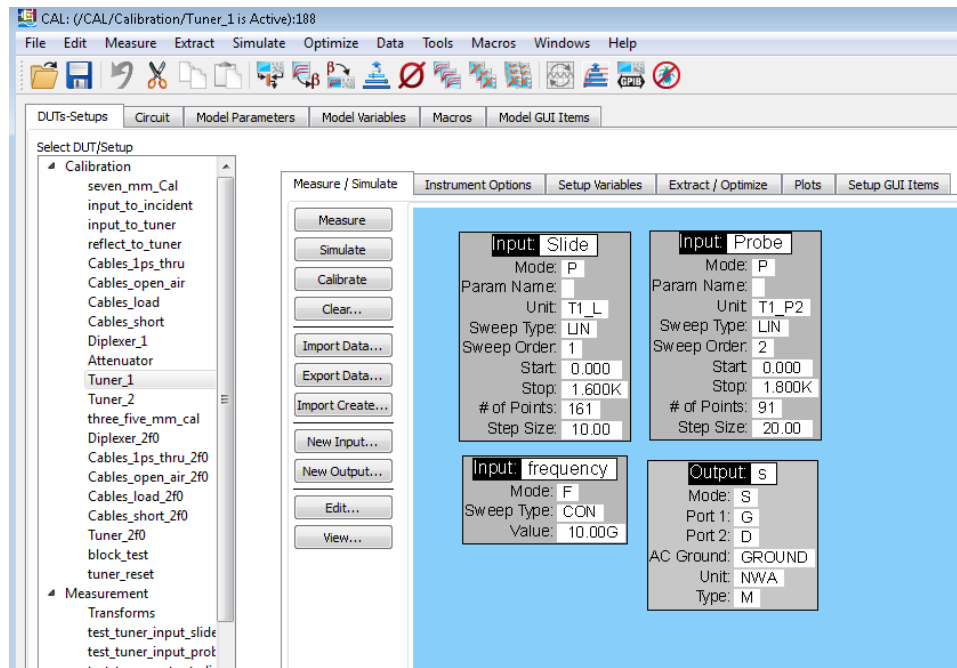


Figure B.12: Tuner calibration inputs and output.

7. Make sure it's running smoothly. It might complain that the settings don't match, that's fine. It's because you're doing a constant frequency instead of a sweep. If the NWA complains about power levels or IF errors, stop the calibration.
8. If it's going ok, great! Go do something else, this will take a while. For the example settings, the calibration will run overnight.
9. When it's finished, check the plots. Figure B.13 is a good example of what you should see. If it's jagged and noisy, you'll need to check the calibration and power settings.
10. Repeat for the output tuner.
11. In each Tuner setup, execute all the transforms.

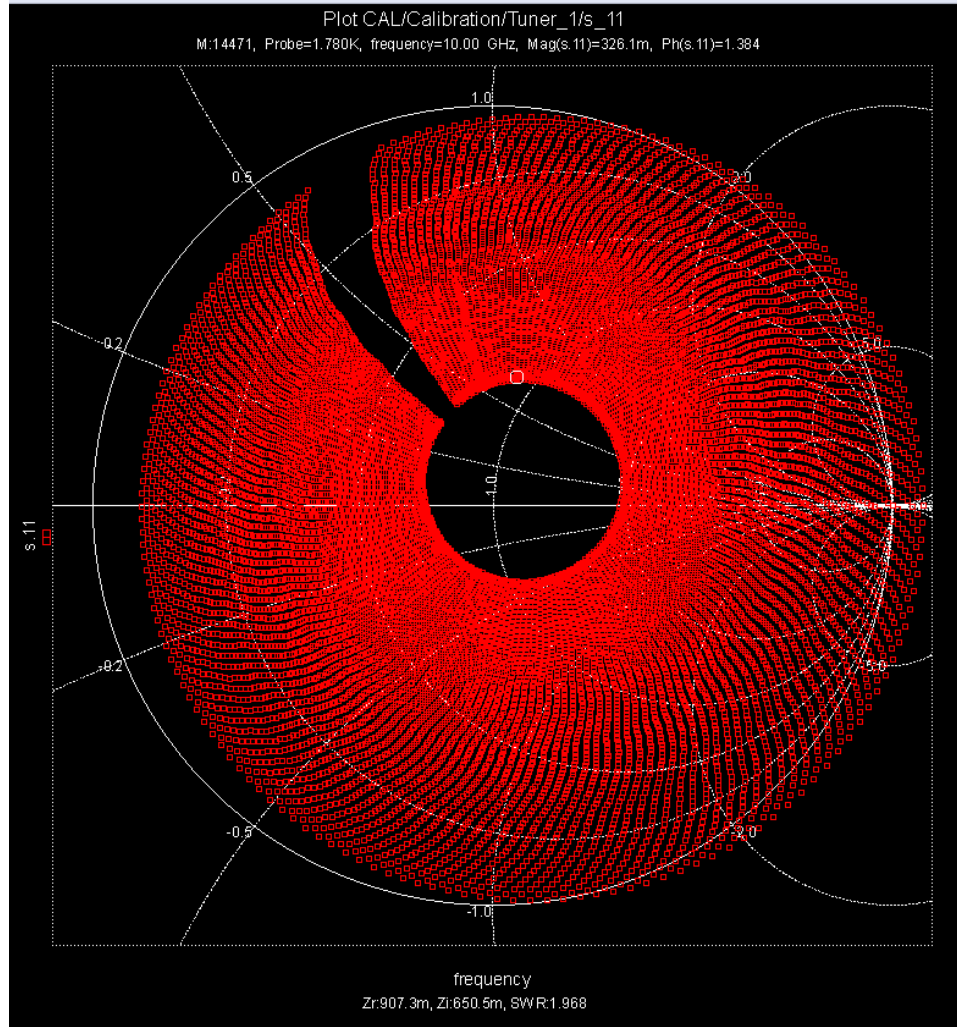


Figure B.13: Tuner calibration S11 plot.

## Second Harmonic Calibration

The second harmonic calibration is done the same way as the fundamental, except that you only need to calibrate the cables, diplexer, and output tuner. This is done by first calibrating the 3.5 mm connectors. Then, all the measurement setups with  $2f_0$  in their name are done exactly as before.

## B.3 Matching and Measurements

Once everything has been calibrated and re-assembled, you can begin taking measurements.

### B.3.1 Setting Variables

1. Probe your device.
2. Use the `Transfer_Curves` setup under `DC_IV` to check that the device works, find its pinch-off, and quiescent voltage (peak of transconductance).
3. Open the `Model Variables` tab. This is where you will enter the bias and tuning parameters. See Figure B.14.

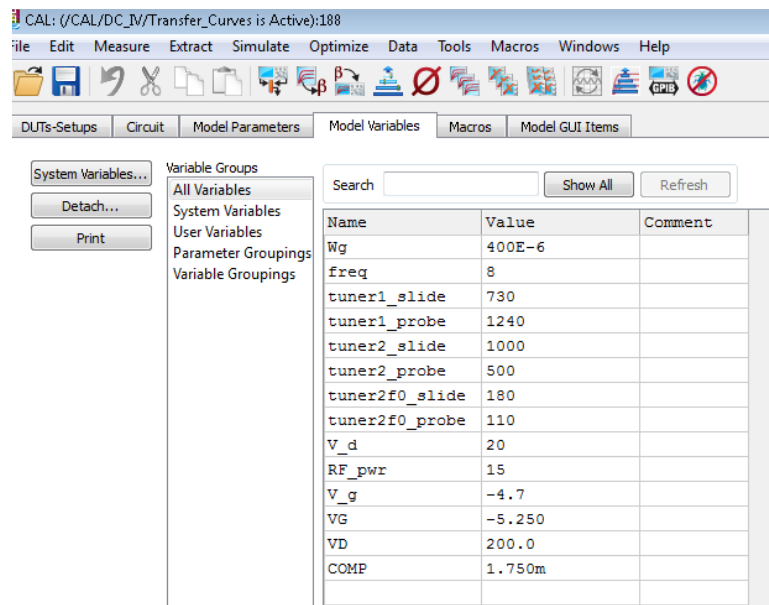


Figure B.14: Model variables tab.



4. Enter the quiescent voltage into the field `V_g`. NOT `VG`, that's used for some macro stuff.
5. Decide what input power and drain bias you want to use for tuning. Enter the power into the `RF_pwr` field and drain bias into the `V_d` field.
6. `Wg` should be the periphery of your device.
7. The `freq` field is the index of the frequency you're using. For example, we calibrated from 9.9 GHz to 10.1 GHz at 0.0125 GHz steps, so 17 points. We calibrated our Tuners at 10 GHz, which is index 8 for that sweep. We set the frequency index to 8 so that when we call the measured S-parameter values for the different pieces, we use the 10 GHz value.
8. If all that looks good, you're ready to start the matching process.

### B.3.2 Input Matching

1. Before you start the matching, set the input and output probes (`tuner1_probe` and `tuner2_probe` in the Model Variables tab) to something like 500 or 1000.
2. Select the first setup for matching, `test_tuner_input_slide`.
3. Verify that the sweeper is set to the correct frequency. Also check that the measurement range and step size are the same as the input tuner calibration. Check that the power meters are all set to Range Auto, or you'll just get a bunch of 9's if the power is too high.
4. Measure.
5. In the Plots tab, open the `Pref_slide` plot.

6. You should see a significant dip in the reflected power. Find the position where the reflected power is lowest by clicking the point. The slide position will be shown at the top of the plot.
7. Enter this value into the `tuner1_slide` field in the Model Variables tab.
8. Now go to the `test_tuner_input_probe` setup and select Measure.
9. Check the reflected power plot and find where the reflected power is lowest. Enter the position into `tuner1_probe`.
10. Repeat the slide and probe measurements until the values don't change.

### B.3.3 Output Matching

1. Select the `test_tuner_output_slide` setup, and hit Measure.
2. View the plot for whichever metric you are trying to maximize (`pae_slide`, or `Pout_slide` for example), find the position that gives you the maximum value, and enter it into the `tuner2_slide` field in the Model Variables tab.
3. Repeat for the probe.
4. If doing second harmonic termination, do the same for the `test_tuner_2f0_slide` and `test_tuner_2f0_probe` setups.
5. Once all the tuners are set, you are ready to run a sweep.

### B.3.4 Power Sweep

1. Select the `power_sweep` setup.

2. This setup will use the tuner settings and drain bias values in the ModelVariables tab. You will need to set the RF power levels, however. This is done in the `sweepPower` input block (Figure B.15. Larger peripherals will need higher power.

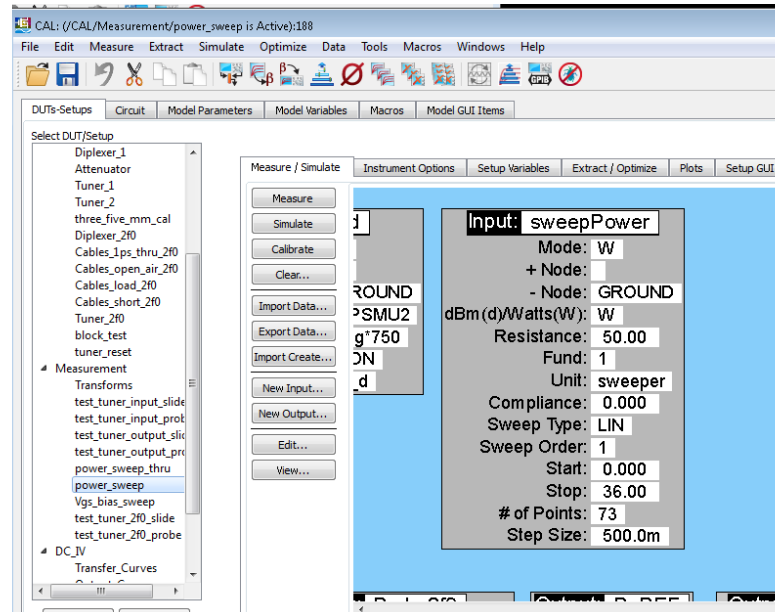


Figure B.15: Power sweep input block.

3. Hit `Measure` when you're ready.
4. The results will be displayed in the `pae_probe` plot in the `Plots` tab. Output power, gain, and PAE will be displayed. See Figure B.16 for an example.
5. You will probably start with a low drain bias, so repeat with different biasing conditions.

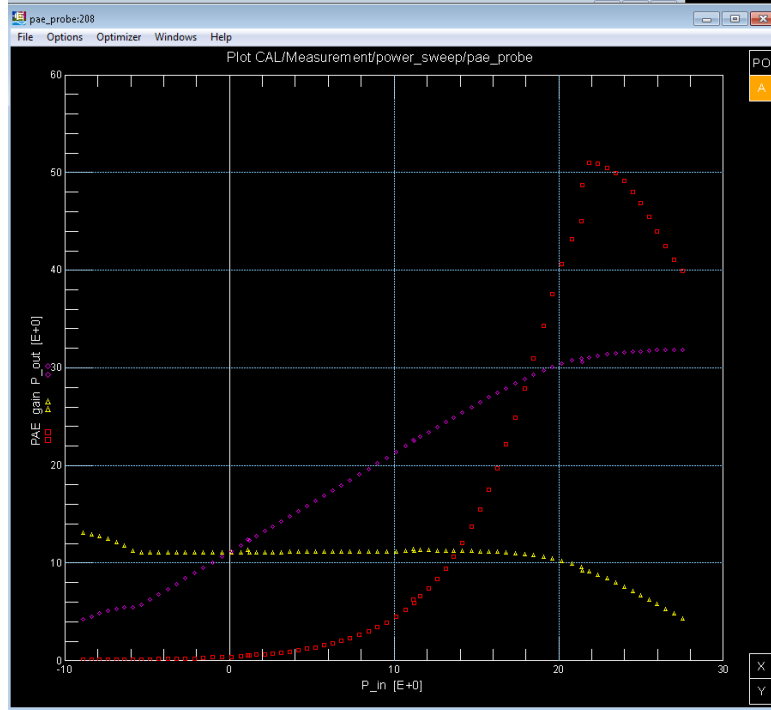


Figure B.16: Power sweep results: gain, PAE, and Pout.

## B.4 Miscellany

### B.4.1 Macros and Transforms

The first two macros in the list are for saving data. The `start_master` macro creates a master file that keeps a summary of the data for all the measurements done on a particular chip. This macro relies on the directory for that chip existing. So make sure it exists.

The `export_data` macro actually writes the data and saves the model for a particular biasing condition. This macro requires that the tuner steps and number of points are correctly hard-coded. If you change the calibration range/step, you have to change it in this macro, as well as the transforms, which leads us

to...

Try not to change the calibration range. Right now, all the calculations for gain/pae/power require that the tuner step and number of points be hard-coded. This can be fixed by making those global variables under `Model Variables`.

## **B.4.2 A Note on Tuner Black Magic**

There are two things you need to be aware of with regard to the Tuners.

First, is that both fundamental tuners are on the controller at address 11. The second harmonic is on the controller at address 12. When you rebuild the instrument list, the driver automatically sets the probe and slide names for the instrument on 12 to the same as those of the instrument on 11. IC-CAP will complain about this, as it should. You will need to go into the GPIB settings, select the instrument at address 12, hit `Configure`, and add an “s” (for “small” tuner) to the end of each of the tuner slide/probe names. See Figure B.17.

The other thing is that sometimes when you rebuild, or lose power, or for whatever reason, the tuners can become “stuck” and won’t respond. You can reset them by first going to each controller and hitting the `Local` button. Then, for each of the Slides (L’s) and Probes (P’s), use the dial to move it around a bit (you should hear it moving). Do the same for the second harmonic tuner.

Once you unstick the tuners, you have to re-home them. This is done by going into IC-CAP and selecting the `tuner_reset` setup (Figure B.18. Click `Calibrate`. IC-CAP will tell you it’s about to calibrate the tuners, just click `Ok`

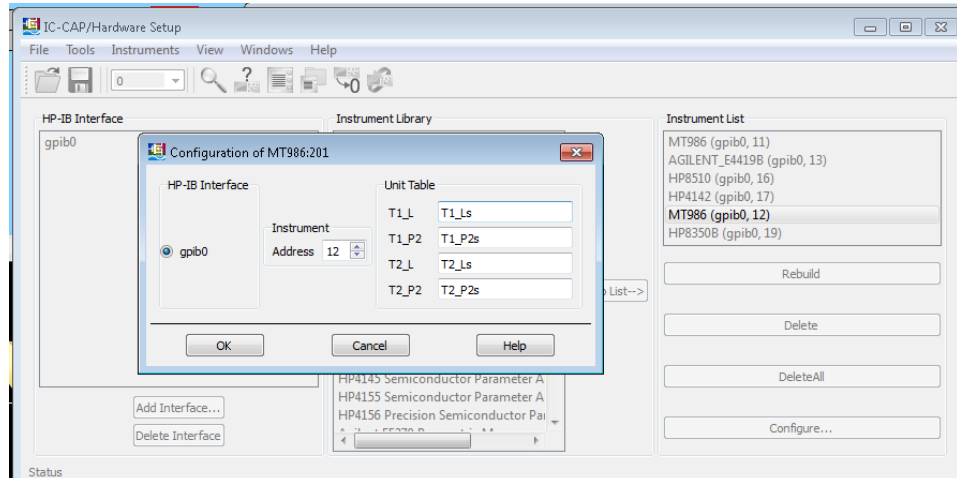


Figure B.17: Renaming the second harmonic tuner slide and probe.

at every prompt. The tuners will go back and find their home positions, and should now work.

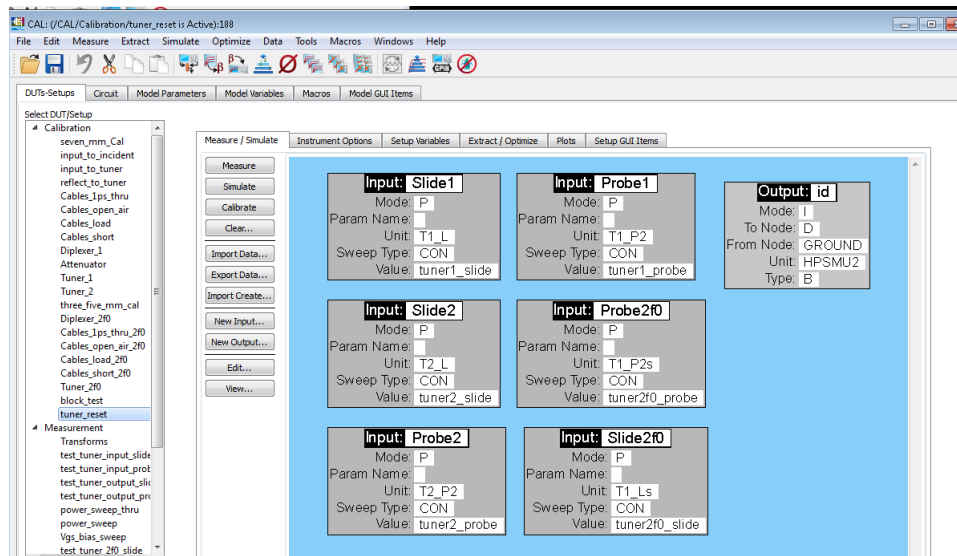


Figure B.18: Tuner reset setup.

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